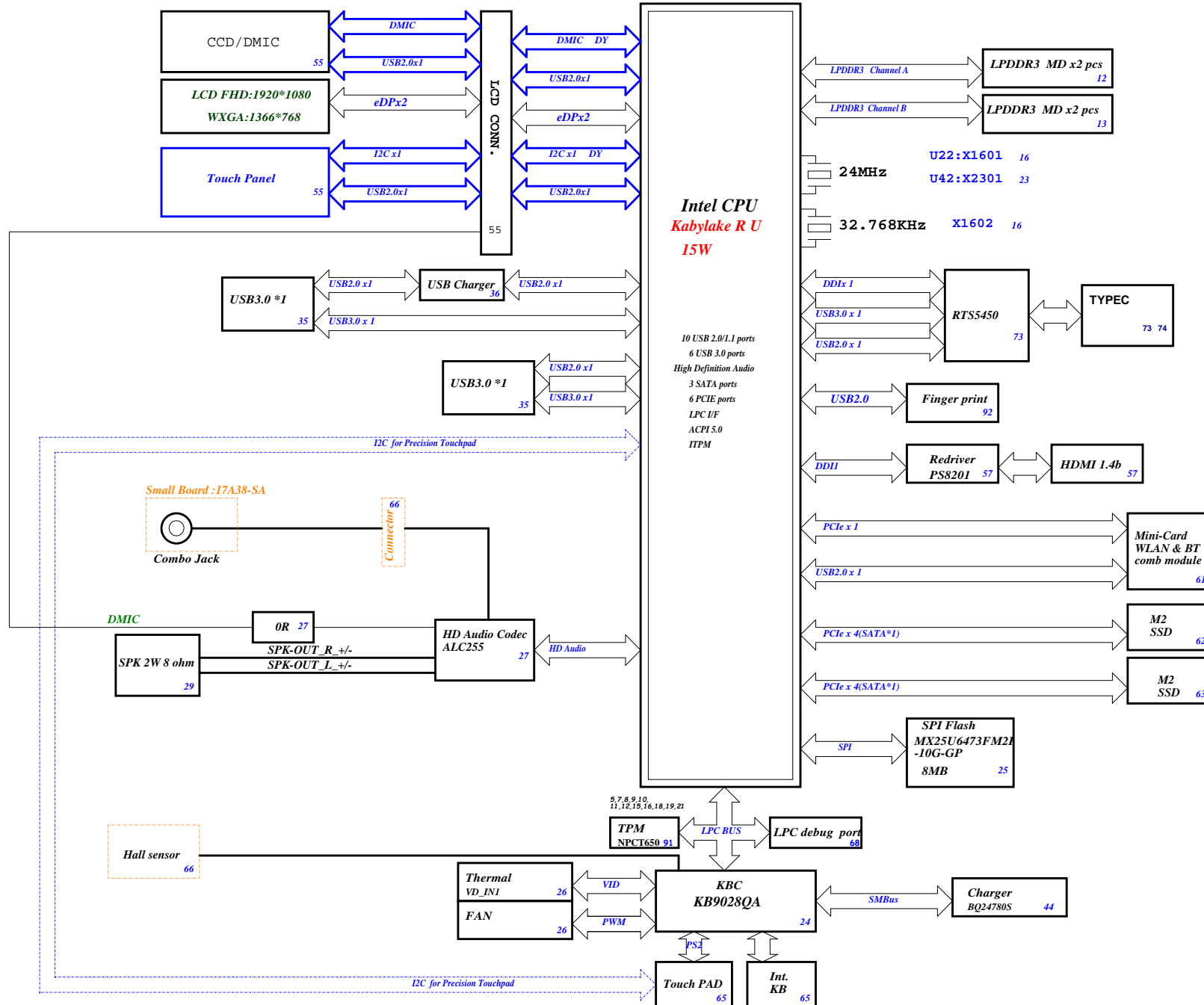


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Schematics Document

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UMA: UMA only installed
DIS: DISCRTE OPTIMUS installed

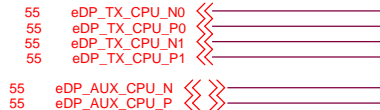
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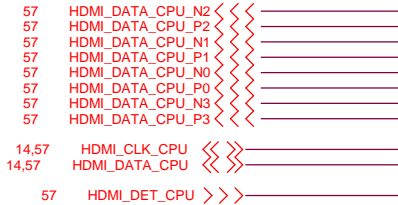


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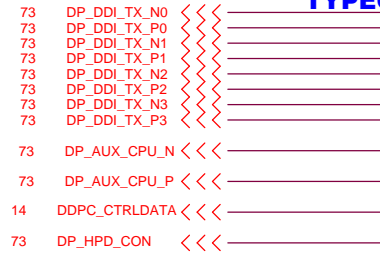
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HDMI



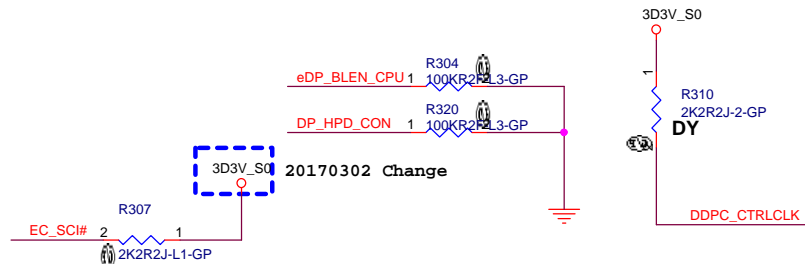
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OTHER



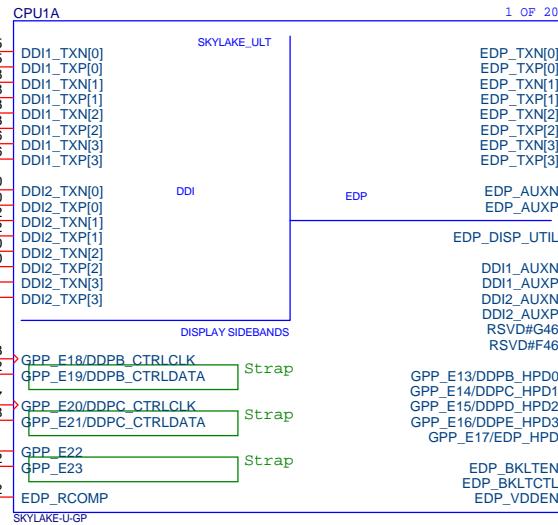
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(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω $\pm 1\%$	Max = 100 mils

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 $\pm 1\%$ Ω resistor.



eDP

eDP

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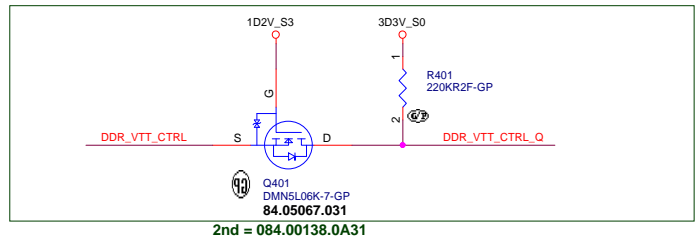
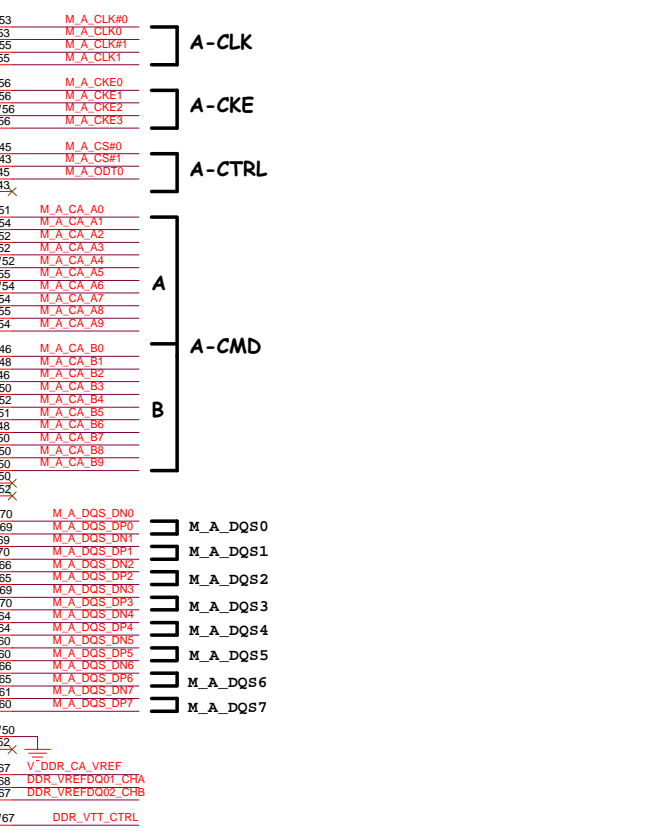
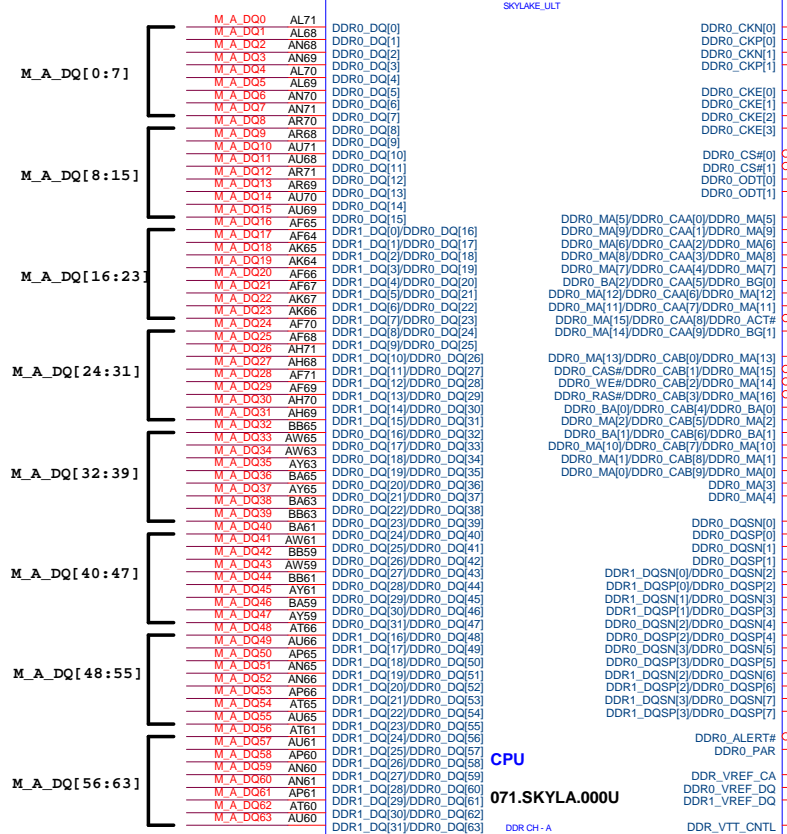
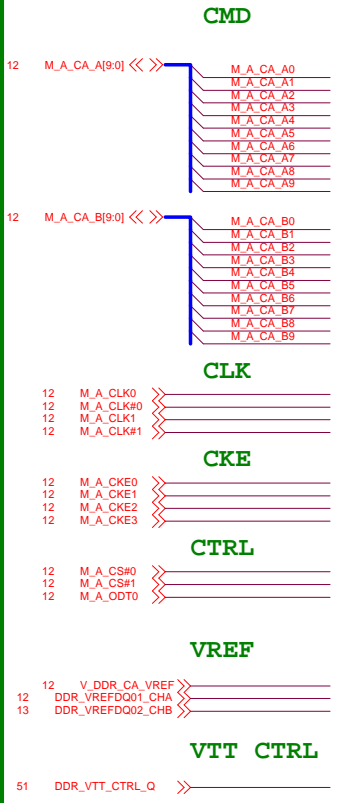
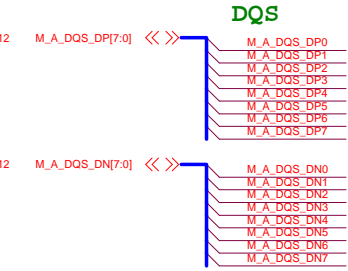
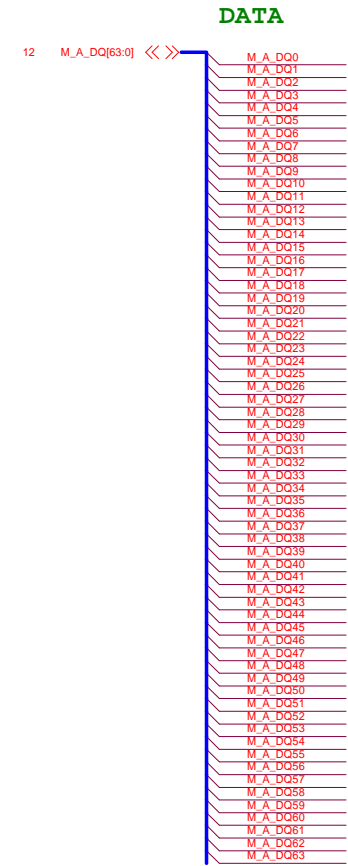
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Main Func = CPU



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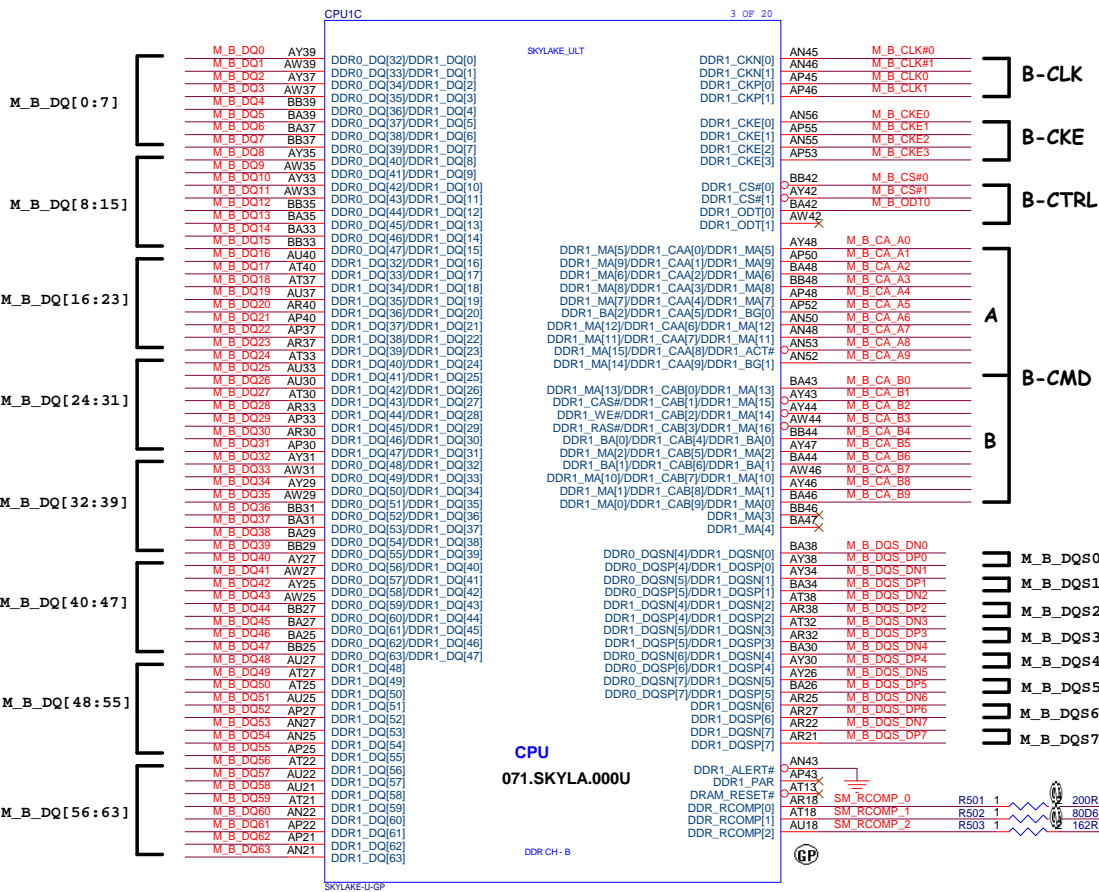
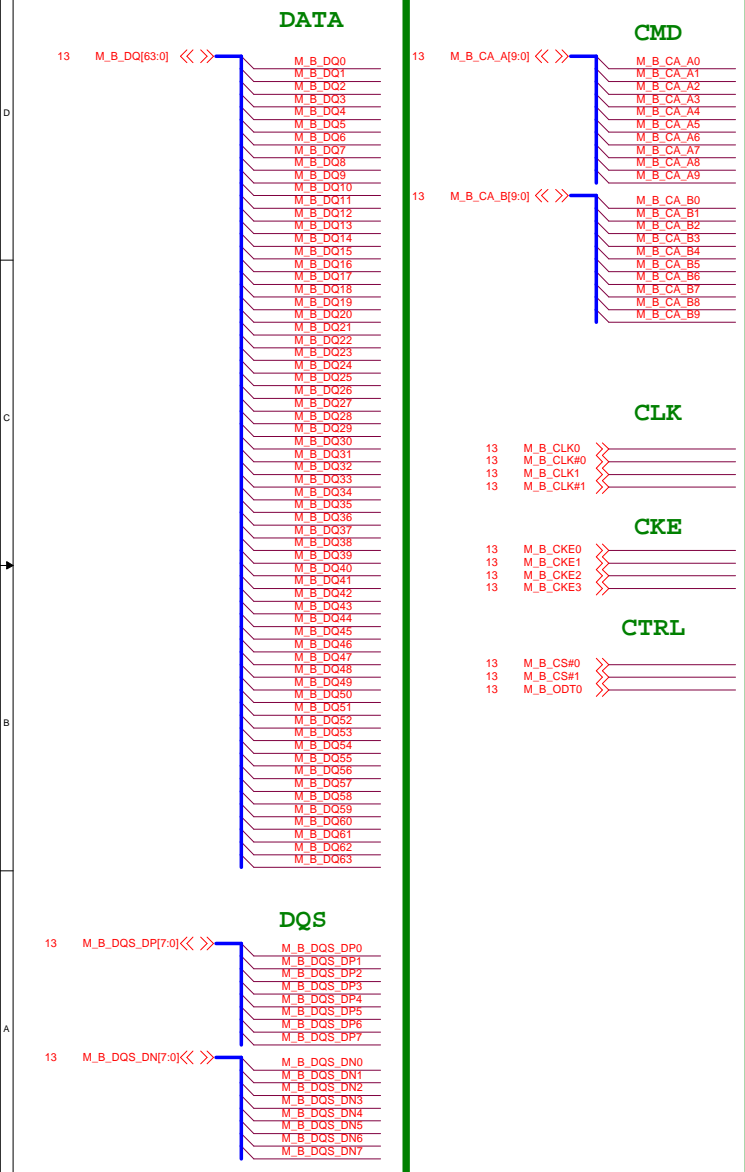
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Main Func = CPU



Signal Group	Region	Layer Route	Reference	Via Count	Trace Width (mils)	Target Impedance (Ω)			Min Trace Spacing (mils)			Max (mils) Length		R (±2 %)	Notes	
						Diff	Single Ended	Tolerance (%)	Diff	Group	Group to Group [1&2]	Byte [1&2]	Region			Total
RCOMP[0]	M	M5/S/L	V5S	5	12-15					20	25		500	500	200	
RCOMP[1]	M	M5/S/L	V5S	5	12-15					20	25		500	500	80.6	
RCOMP[2]	M	M5/S/L	V5S	5	12-15					20	25		500	500	162	



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Main Func = PCH

DETECT&RESET

55 TOUCH_DET# <<=

25 RTC_DET# <<=

DEBUG PORT

68 LPSS_UART2_RXD >>=

68 LPSS_UART2_TXD >>=

I2C

65 PM_TP_DATA >>=

65 PM_TP_CLK >>=

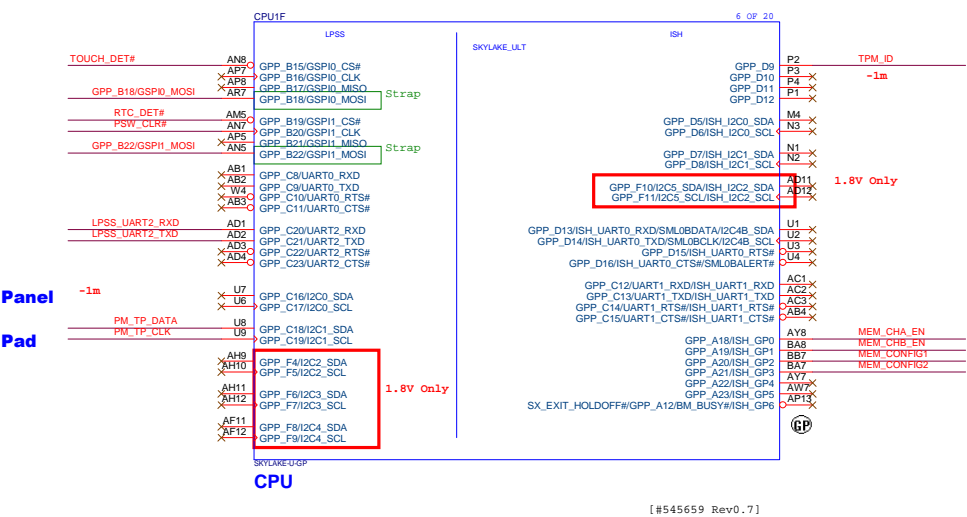
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14 GPP_B18/GSP10_MOSI <<=

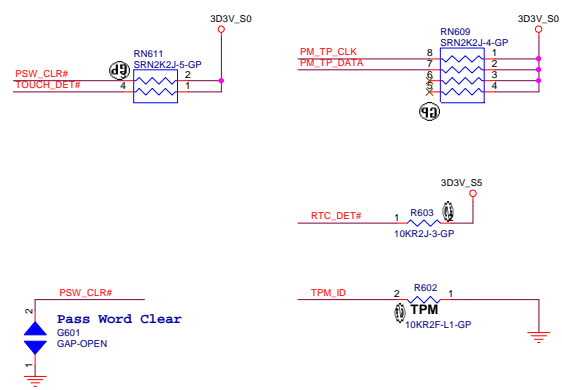
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Touch Panel

Touch Pad

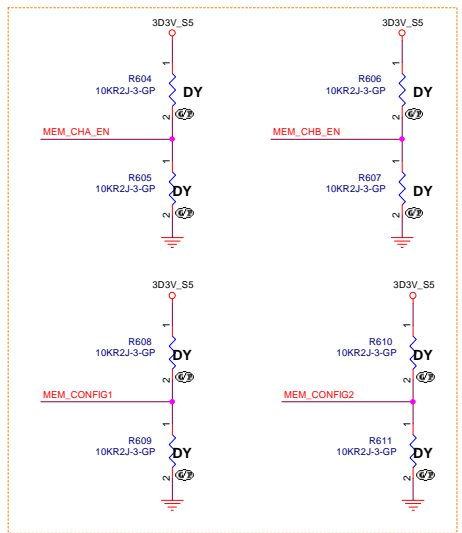


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GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDW_3p3	3.3V



Vender	Config4 (GPIO_A19)	Config3 (GPIO_A18)	Config2 (GPIO_A21)	Config1 (GPIO_A20)	MF.PN	Wistron PN	Capacity	Total Capacity
SK HYNIX	0	0	0	0	H9CCNNN8GTALAR-NUD LF+HF	KN.1GB0G.030	1GB	4GB
SK HYNIX	0	0	0	1	H9CCNNN8LTBLAR-NUD LF+HF	KN.0160G.006	2GB	8GB
SK HYNIX	0	0	1	0	H9CCNNN8BTALAR-NUD LF+HF	KN.2GB0G.053	2GB	8GB
MICRON SG	0	0	1	1	MT52L256M32D1PF-107 LF+HF	KN.8GB04.016	1GB	4GB
MICRON SG	0	1	0	0	MT52L512M32D2PF-107 LF+HF	KN.01604.002	2GB	8GB
MICRON SG	0	1	0	1	MT52L1G32D4PG-107 LF+HF	KN.4GB04.014	4GB	16GB
SK HYNIX	0	1	1	0	H9CCNNN8CLGALAR-NUD LF+HF	KN.4GB0G.048	4GB	16GB
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

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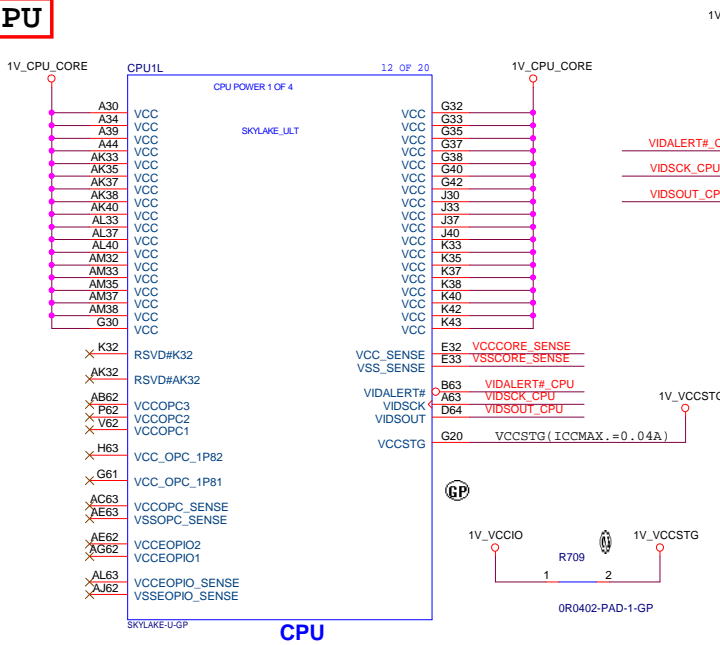
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Main Func = CPU

SVID

- 46 SVID_ALERT#_CPU <<< —
- 46 SVID_CLK_CPU <<< —
- 46 SVID_DATA_CPU <<< —
- 46 VCCCORE_SENSE <<< —
- 46 VSSCORE_SENSE <<< —



Layout Note:

- 1. Place close to CPU
- 2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
- 3. Length match<25mil

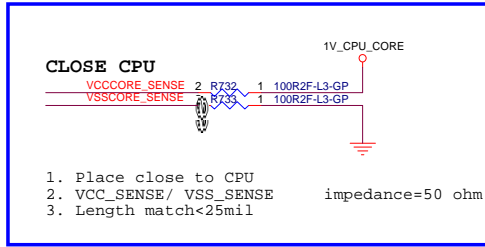
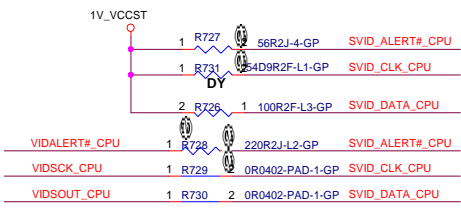


Figure 10-7. Routing Illustration for SVID Topology

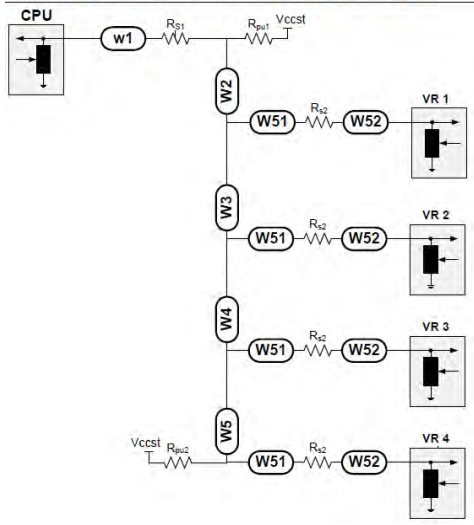


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R _{Pu1} [Ω]	R _{Pu2} [Ω]	R _{S1} [Ω]	R _{S2} [Ω]	VCC _{ST} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

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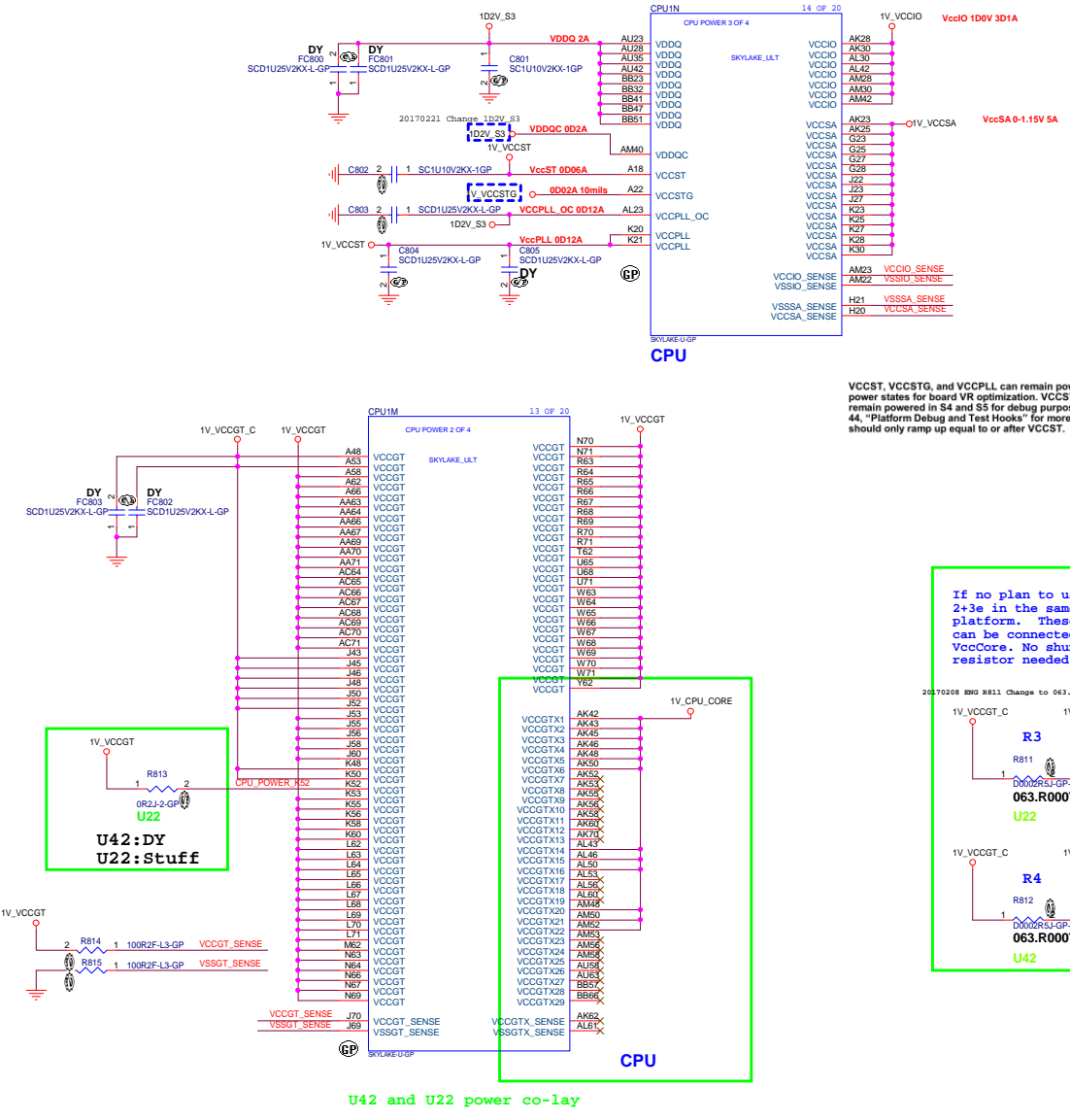
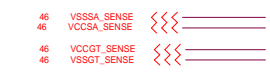
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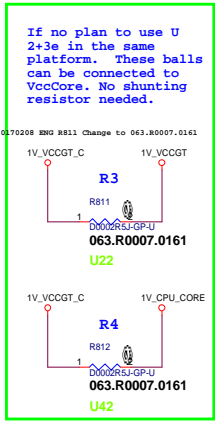
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Main Func = CPU



VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization. VCCSTG may also remain powered in S4 and S5 for debug purposes. Refer to Chapter 44, "Platform Debug and Test Hooks" for more details. VCCSTG should only ramp up equal to or after VCCST.



KBL U42 Board Compatibility with KBL U22/23e

• 4 Rshunts Required

- R1 – between VCCGTU VR and VCCGTU
- R2 – between VCCGTU and VCCCORE
- R3 – between VCCGT and VCCGT VR
- R4 – between VCCGT and VCCCORE

- Stuff R1 and R3 when U22 or U23e mount on board
- Stuff R2 and R4 and de-pop R1 and R3 when U42 mount on board

U22	R1	X	R3	X
U42	X	R2	X	R4

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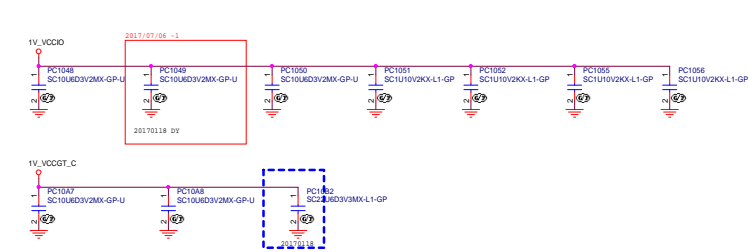
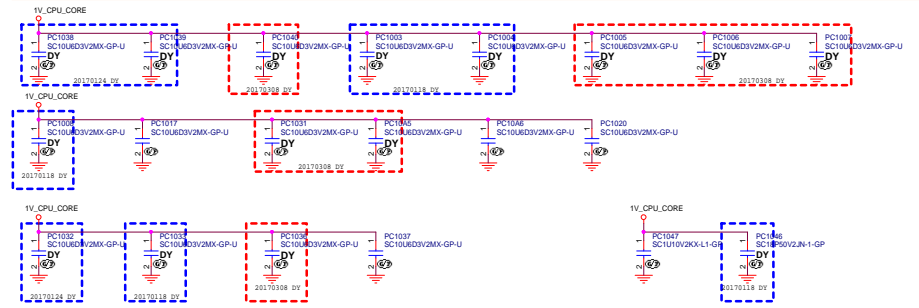
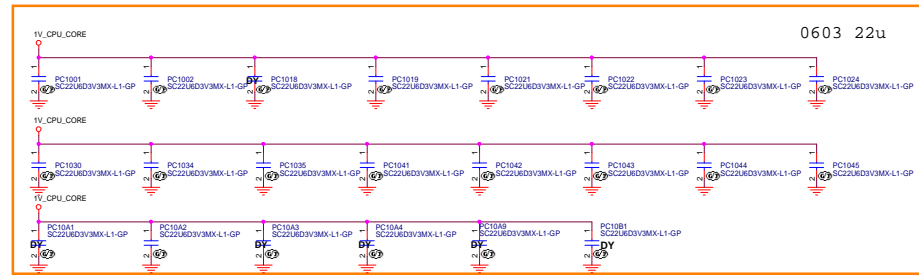
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Blanking

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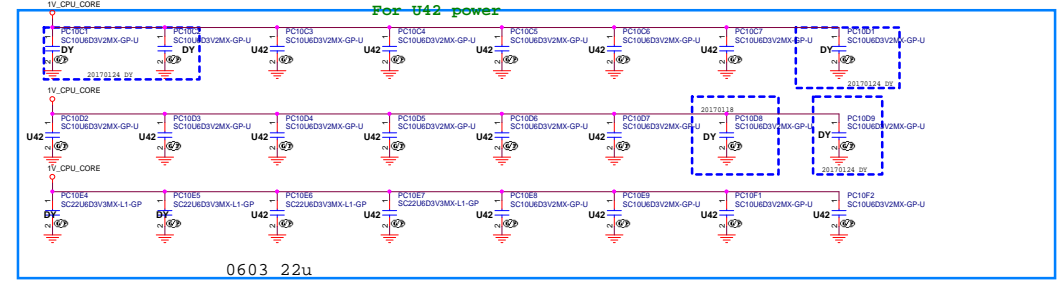
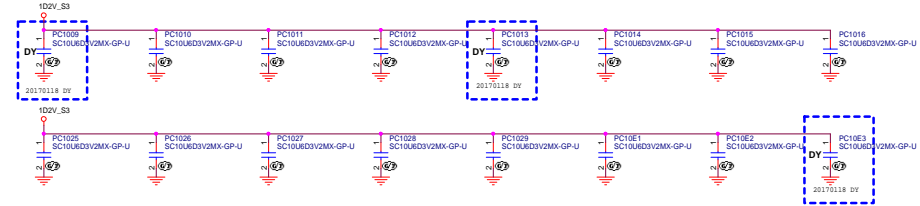
Main Func = CPU



1V_CPU_CORE

U22 0603 22uF *22 , 0402 10uF*11 , 1uF*1

U42 0603 22uF *4 , 0402 10uF*15



0603 22u

Power Layout



48.1.3 Kaby Lake U Compatible Design Recommendation

48.1.3.1 KBL-R U 4+2 / KBL U 2+2 Design Recommendation

Table 48-3. Bulk Decoupling Example (KBL-R U42/KBL U22)

Bulk Decoupling Locations	Example - U 4+2	Example - U 2+2	Notes
Vcc Power Plane at VR output	2x 220 uF (@4.5mΩ ESR)	1x 220 uF (@4.5mΩ ESR)	Placed at primary side near to VR output
Vcc _{IO} Power Plane at VR output	2x 220 uF (@4.5mΩ ESR)	1x 220 uF (@4.5mΩ ESR)	Placed at backside side near to VR output
V _{DDQ} Power Plane at VR output	2x 47 uF 0805	2x 47 uF 0805	Placed at primary side near to VR output
V _{DDQ} Power Plane at VR output	2x 47 uF 0805	2x 47 uF 0805	Placed at primary side near to VR output
V _{DDQ} Power Plane at VR output	2x 47 uF 0805	2x 47 uF 0805	Placed at primary side near to VR output
V _{DDQ} Power Plane at VR output	2x 47 uF 0805	2x 47 uF 0805	Placed at primary side near to VR output
V _{DDQ} Power Plane at VR output	2x 47 uF 0805	2x 47 uF 0805	Placed at primary side near to VR output
V _{DDQ} Power Plane at VR output	2x 47 uF 0805	2x 47 uF 0805	Placed at primary side near to VR output
V _{DDQ} Power Plane at VR output	2x 47 uF 0805	2x 47 uF 0805	Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

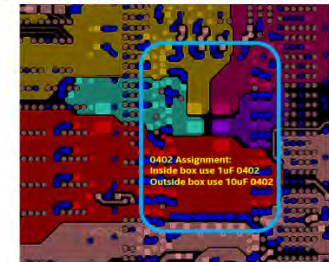
Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 1 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	31x 1 uF 0402 or 0201		Refer to diagram in Note 4 below for placement recommendation of 0402 caps
		9x 22 uF 0603	Place as close to the package as possible
		8x 47 uF 0805 (6.3V)	
		8x 10 uF 0402	
Vcc/Vcc _{IO}	5x 1 uF 0402 or 0201		Place as close to the package as possible
Vcc _{GT}	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
		7x 22 uF 0603	Place as close to the package as possible
		3x 47 uF 0805 (6.3V)	

Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 2 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc _{SA}	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
Vcc _{IO}		6x 10 uF 0402	Place as close to the package as possible
V _{DDQ}		4x 1 uF 0402	Place as close to the package as possible
		4x 10 uF 0402	Place as close to the package as possible
		3 x 22 uF 0603	Place as close to the package as possible
V _{DDQ}		1 x 10 uF 0402	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQ pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example shown in Figure 48-3. The 0402 cap to VDDQ BGA routing should not exceed 4mm (max). RVP design uses trace L=450mil, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.
Vcc _{LL}		1x 1 uF 0402	Place as close to the package as possible.
Vcc _{LL_OC}		1x 1 uF 0201	Do not route Vcc _{LL} , Vcc _{LL_OC} , Vcc _{IO} closest adjacent layer over any power net other than ground.
Vcc _{ST}		1x 1 uF 0402	For Vcc _{ST} Refer to Figure 48-2 for additional routing details for Vcc _{ST} & Vcc _{STG} .

Notes:
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth > 250kHz e.g., 1MHz switching VR
2. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps > Power source
3. Due to the difference between the package designs, KBL U 2+2 design requires more on-board decoupling in order to maintain the same guideline.
4. Diagram of placement for 0402 backside caps for CPU decoupling.

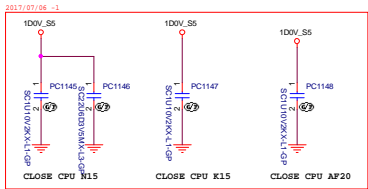


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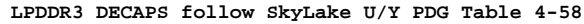
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Modify by power Jason
2017/0630

U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1m(2)	30A (30)	200m/30us	1X0.15uH	2X330f/9mH	30X22
								Or	1X330f/9mH	36X22
	GT	750kHz	40A (31A)	18A (18A)	3.1m(2)	38A (38)	70m/10us	1X0.15uH	2X330f/9mH	24X22
								Or	1X330f/9mH	36X22
	SA	750kHz	6A (5A)	6A (4A)	10.3m(2)	4A (30)	200m/30us	1X0.4uH	None	5X22

DATA

[illegible][illegible]

Layout Note: Place these Caps near CHA Terminations

The diagram illustrates the placement of decoupling capacitors near CHA terminations. A central block labeled 'VTT DECAPS' contains four capacitors: C1241, C1243, C1244, and C1245. These capacitors are connected to a common VTT node. To the left, a capacitor C1241 is connected to a VTT node and a termination point labeled 'd0-7562X003R11241'. To the right, a capacitor C1245 is connected to a VTT node and a termination point labeled 'd0-7562X003R11245'. All capacitors are connected to ground.

CHA/CHB_LPDDR3_VREFCA

10kV_S3

R1209
BK2R2F-1-GP

N

M_VREF_CA_DIMMA

4 V_DDR_CA_VREF

R1206
10k

SD11R2F-GP

1239

R1208
BK2R2F-1-GP

N

10kV_S3

R1207
10k

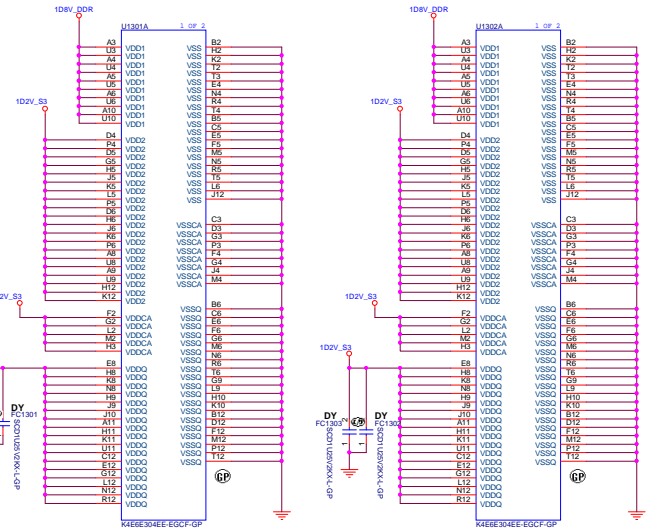
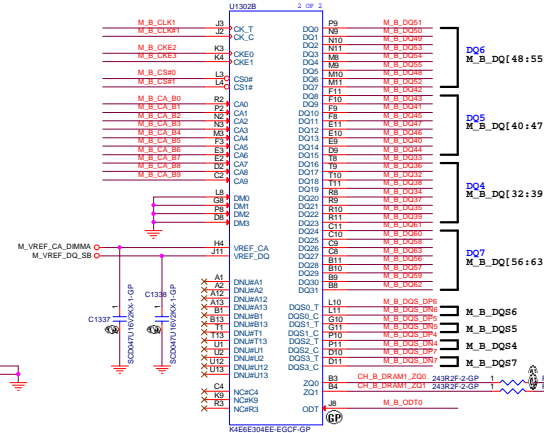
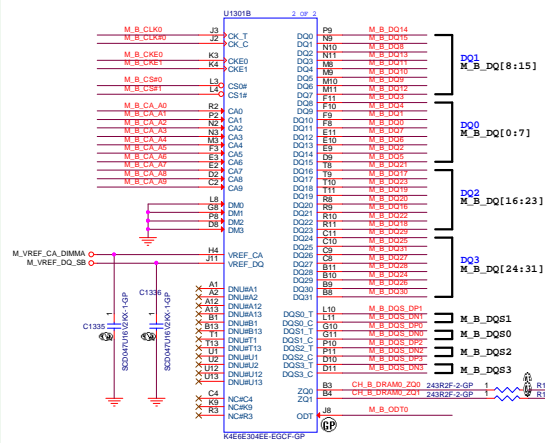
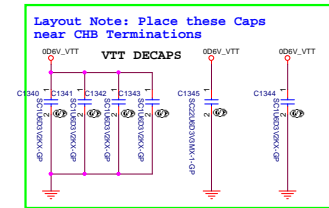
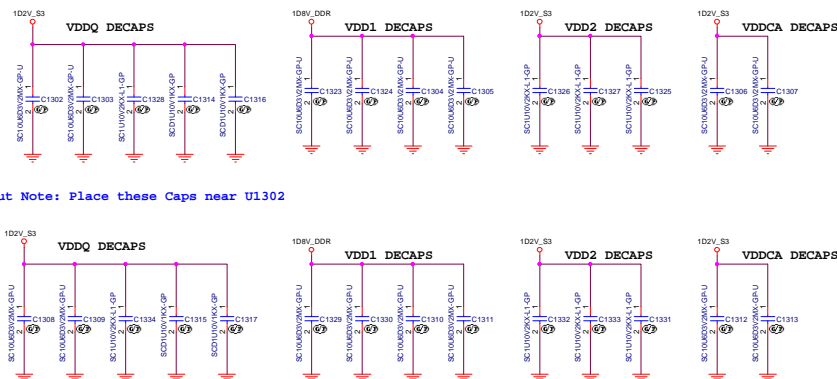
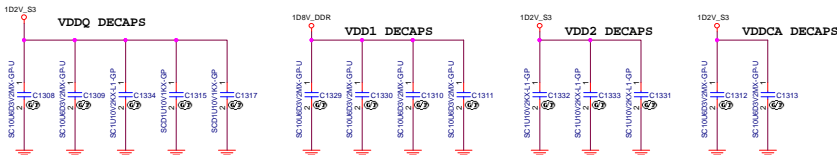
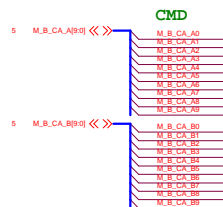
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VREF #2

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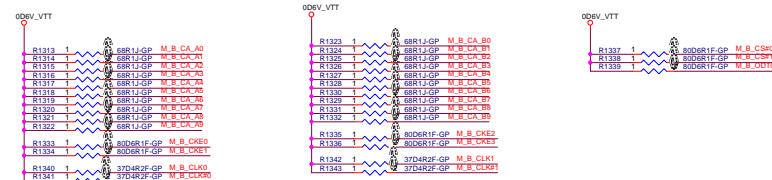
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M.B.DQ14		M.B.DQ14
M.B.DQ15		M.B.DQ15
M.B.DQ16		M.B.DQ16
M.B.DQ17		M.B.DQ17
M.B.DQ18		M.B.DQ18
M.B.DQ19		M.B.DQ19
M.B.DQ20		M.B.DQ20
M.B.DQ21		M.B.DQ21
M.B.DQ22		M.B.DQ22
M.B.DQ23		M.B.DQ23
M.B.DQ24		M.B.DQ24
M.B.DQ25		M.B.DQ25
M.B.DQ26		M.B.DQ26
M.B.DQ27		M.B.DQ27
M.B.DQ28		M.B.DQ28
M.B.DQ29		M.B.DQ29
M.B.DQ30		M.B.DQ30
M.B.DQ31		M.B.DQ31
M.B.DQ32		M.B.DQ32
M.B.DQ33		M.B.DQ33
M.B.DQ34		M.B.DQ34
M.B.DQ35		M.B.DQ35
M.B.DQ36		M.B.DQ36
M.B.DQ37		M.B.DQ37
M.B.DQ38		M.B.DQ38
M.B.DQ39		M.B.DQ39
M.B.DQ40		M.B.DQ40
M.B.DQ41		M.B.DQ41
M.B.DQ42		M.B.DQ42
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M.B.DQ55		M.B.DQ55
M.B.DQ56		M.B.DQ56
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M.B.DQ58		M.B.DQ58
M.B.DQ59		M.B.DQ59
M.B.DQ60		M.B.DQ60
M.B.DQ61		M.B.DQ61
M.B.DQ62		M.B.DQ62
M.B.DQ63		M.B.DQ63

[illegible][illegible]

```

5    M_B_CLK0
5    M_B_CLK#0
5    M_B_CLK1
5    M_B_CLK#1

```



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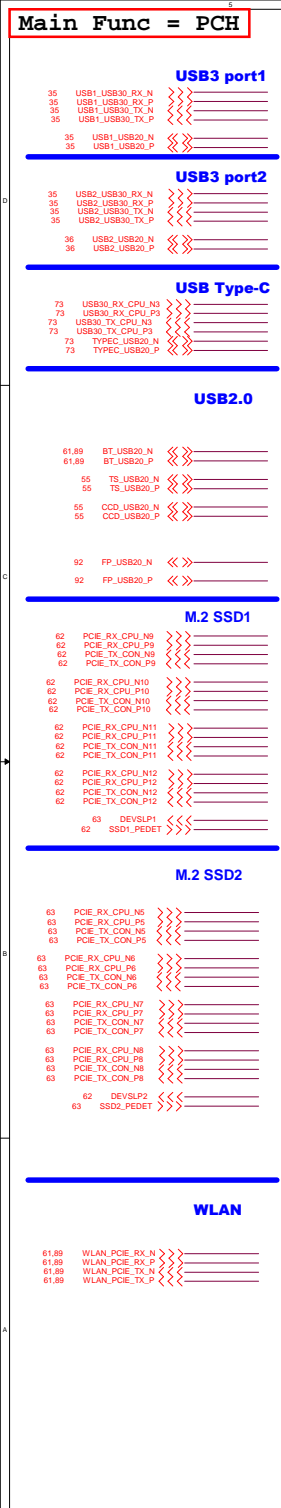
Description	Top Swap Override	Reserved	Reserved	Reserved	TLS Confidentiality	eSPI or LPC	Reserved
GPIO	GPP_B14	SPI0_MOSI	SPI0_IO2	SPI0_IO3	GPP_C2	GPP_C5	GPP_B23
Schematic							
High	Enable				Enable	eSPI	
Low	Disable				Disable	LPC	
	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-down	internal pull-down	internal pull-down

Signal	Usage	When Suspended	Comments
DDPOE_CTR_DATA# / GPP_C32	Display copy of collected	Rising edge of PCH_PWBCK	<p>This signal has a weak internal pull-down.</p> <ul style="list-style-type: none"> 0 = Port is not detected. 1 = Port is detected. <p>Notes:</p> <ul style="list-style-type: none"> 1. The internal pull-down is disabled after FLTRST# de-asserts. 2. This signal is in the primary well.
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWBCK	<p>The signal has a weak internal pull-down.</p> <ul style="list-style-type: none"> 0 = Disable "Top Swap" mode. (Default) 1 = Enable "Top Swap" mode. This inverts an address on access to SPI and Firmware Hub, so the processor believes it has been swapped. This is useful to connect the original boot block. PCH will invert A16 (default) for cycles going to the upper 16K of 24K in the FWB or the appropriate address lines (A16, A17, or A18) as selected in top swap block size soft strap (handled through FITC). <p>Notes:</p> <ul style="list-style-type: none"> 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Gsub, Device 3, function0, offset CCH, bit 4). 4. This signal is in the primary well.
SMALERT# / GPP_C2	TLS Confidentiality	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <ul style="list-style-type: none"> 0 = Disable Intel® Cryptographic Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel® Cryptographic Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel APT with TLS and Intel SBA (Small Business Advantage) with TLS. <p>Notes:</p> <ul style="list-style-type: none"> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SMLOALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <ul style="list-style-type: none"> 0 = LPC is selected for EC. 1 = eSPI is selected for EC. <p>Notes:</p> <ul style="list-style-type: none"> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
HD Audio					
HDA_3V3	Primary	Driven Low	Driven Low	Driven Low	OFF
HDA_5V0	Primary	Internal Pull-down	Driven Low	Internal Pull-down	OFF
HDA_5V0	Primary	Internal Pull-down	Driven Low	Driven Low	OFF
IO					
IO_3V3	Primary	Internal Pull-down	Internal Pull-down	Internal Pull-down	OFF

Signal Name	Pin Plane	During Reset	Immediately After Reset	50/50/50	Off	Deep SW
AP0_CLE	Primary	Driven Low (See Note 3)	Driven Low	Driven Low	Off	Off
AP0_M0E0	Primary	Internal Pull-up/ Pull-downs (See Note 3 & 2)	Driven Low	Driven Low	Off	Off
AP0_M0E0	Primary	Internal Pull-up (See Note 3)	Internal Pull-up	Internal Pull-up	Off	Off
AP0_CSLE	Primary	Driven High (See Note 3)	Driven High	Driven High	Off	Off
AP0_CSE	Primary	Internal Pull-up (See Note 3)	Driven High	Driven High	Off	Off
AP0_CSLE [1:3]	Primary	Internal Pull-up (See Note 3)	Internal Pull-up	Internal Pull-up	Off	Off
AP1_CLE	Primary	Undriven	Undriven	Undriven	Off	Off
AP1_M0E0	Primary	Undriven	Undriven	Undriven	Off	Off
AP1_M0E0	Primary	Undriven	Undriven	Undriven	Off	Off
AP1_CSE	Primary	Undriven	Undriven	Undriven	Off	Off
AP1_CSLE [1:3]	Primary	Undriven	Undriven	Undriven	Off	Off

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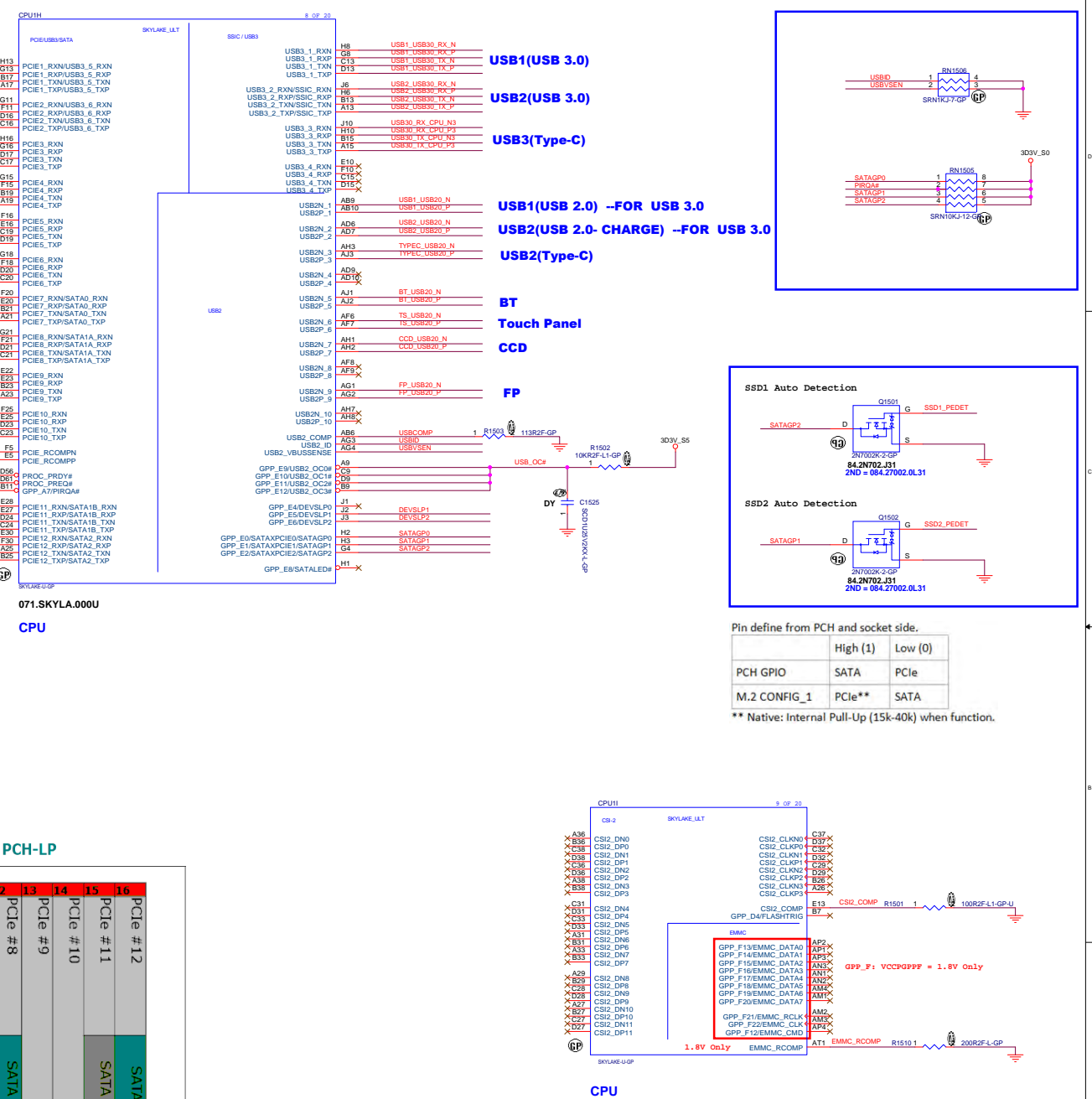
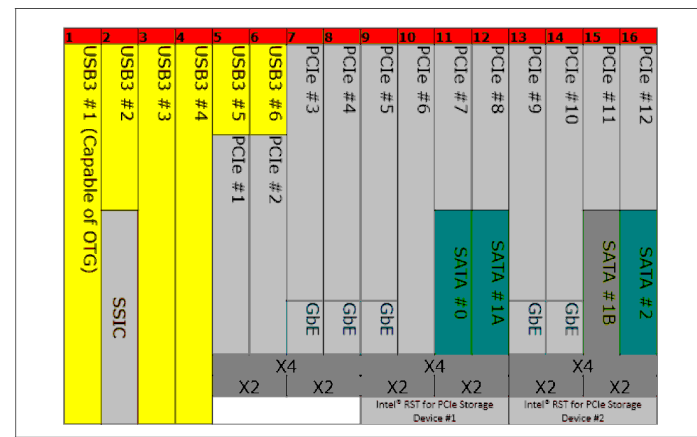
Layout Note:

1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)

Note: Must maintain low DC resistance routing (<0.1 ohm).

2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

Figure 11-1. High Speed I/O (HSIO) Lane Multiplexing in KBL R U PCH-LP

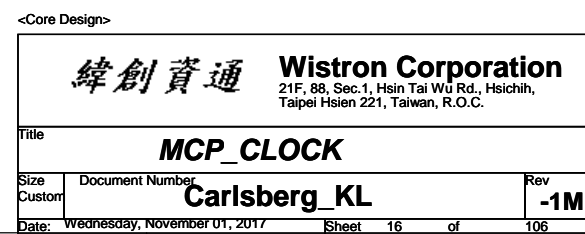
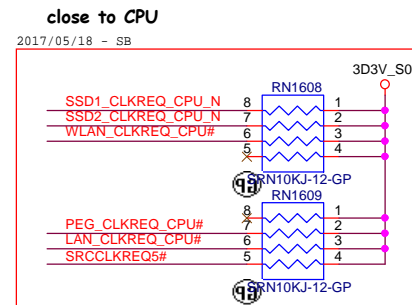
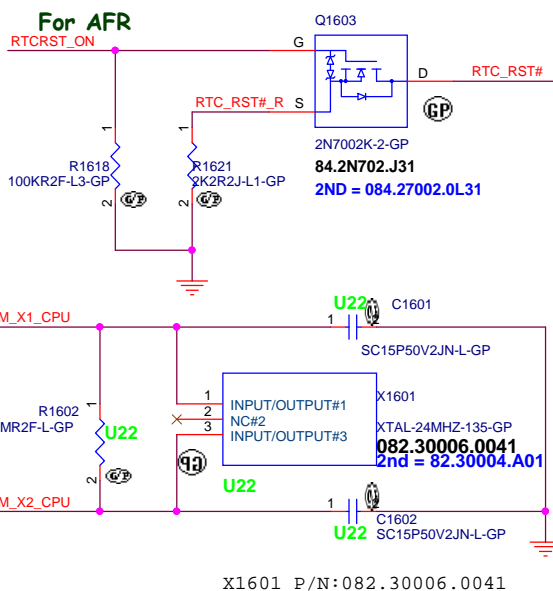


Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

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Main Func = PCH

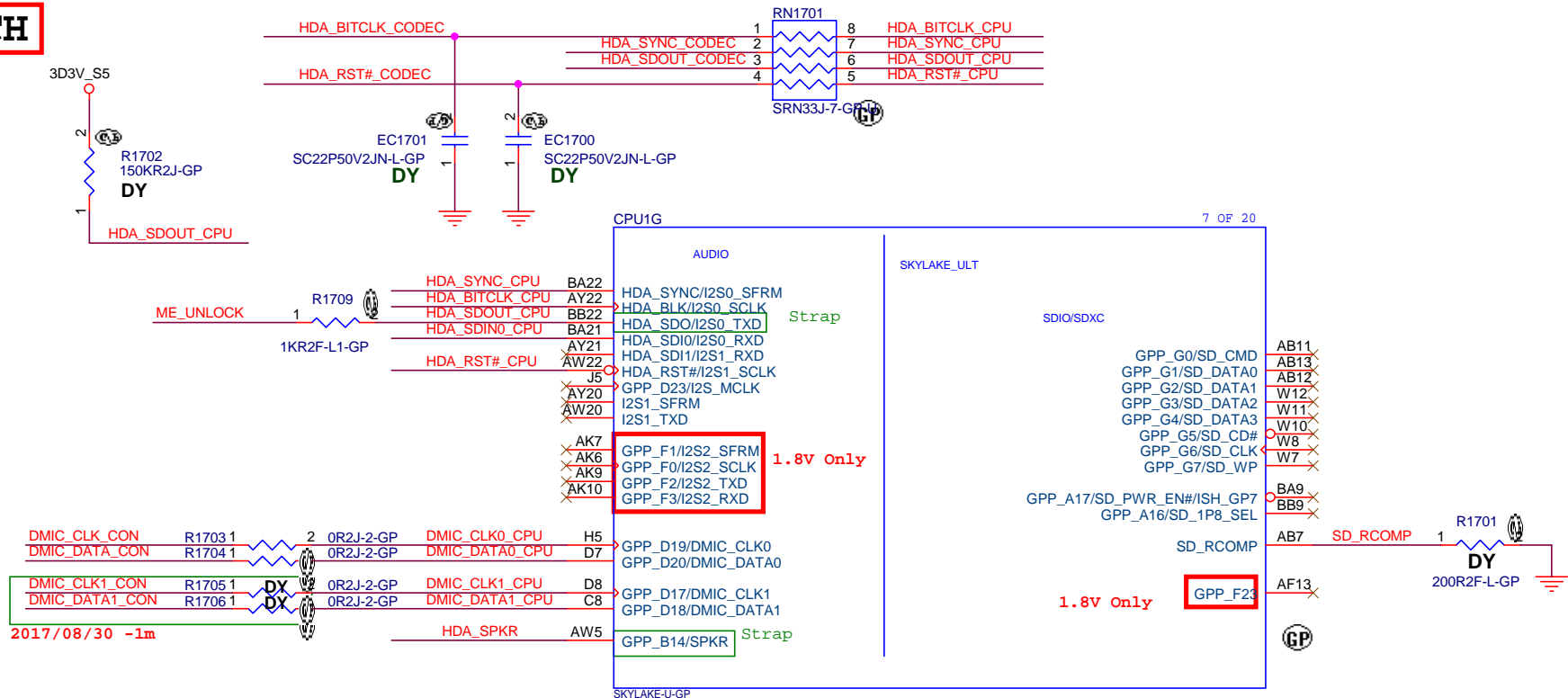
Audio Code

27 HDA_SYNC_CODEEC
27 HDA_BITCLK_CODEEC
27 HDA_SDOUT_CODEEC
27 HDA_SDIN0_CPU
14,27 HDA_SPKR
27 HDA_RST#_CODEEC

24 ME_UNLOCK <<<

DMIC

27,55 DMIC_DATA_CON
27,55 DMIC_CLK_CON
55 DMIC_DATA1_CON
55 DMIC_CLK1_CON



18.3 Terminating Unused SDXC Signals

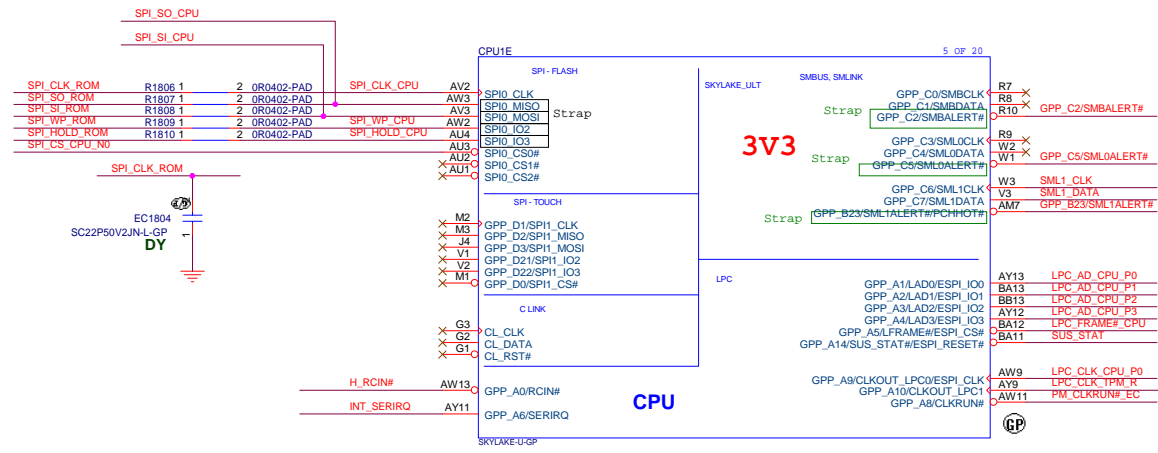
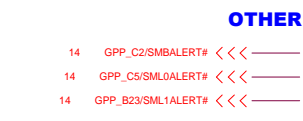
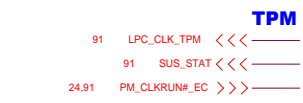
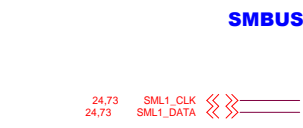
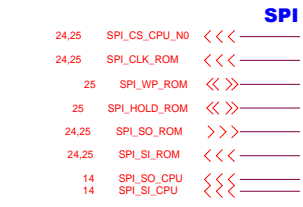
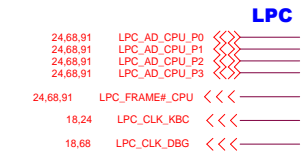
SDXC signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDXC interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

Additionally, if SDXC interface is not used, the SD_RCOMP pin does not need to be connected to a RCOMP resistor.

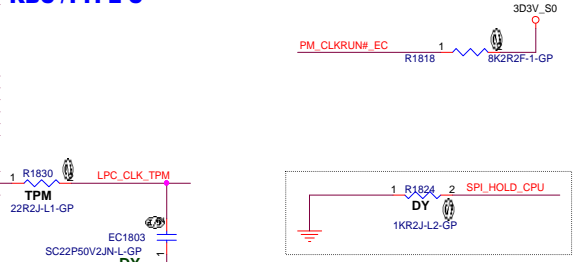
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Title CPU_(AUDIO/SDIO/SDXC)			
Size Custom	Document Number	Rev	
	Carlsberg_KL	-1M	
Date: Wednesday, November 01, 2017	Sheet 17	of 106	

Main Func = PCH



KBC /TYPE-C



Processor Interface	RCIN#	Keyboard Controller Reset Processor: The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the processor other sources of INIT#. When the processor detects the assertion of this signal, INIT# is generated for 16 PCI clocks.
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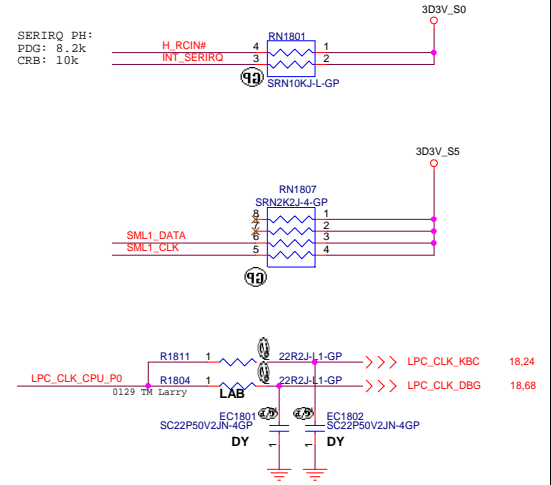
20.9 Serial Interrupt

The PCH supports a serial IRQ scheme. This allows a single signal to be used to report interrupt requests. The signal used to transmit this information is shared between the PCH and all participating peripherals. The signal line, SERIRQ, is synchronous to 24 MHz CLKOUT_LPC, and follows the sustained tri-state protocol that is used by all PCI signals. This means that if a device has driven SERIRQ low, it will first drive it high synchronous to PCI clock and release it the following PCI clock. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S – Sample Phase**, Signal driven low
- **R – Recovery Phase**, Signal driven high
- **T – Turn-around Phase**, Signal released

The PCH supports a message for 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0–1, 3–15), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20–23).

Note: IRQ14 and IRQ15 are special interrupts and maybe used by the GPIO controller when it is running GPIO driver mode. When the GPIO controller operates in GPIO driver mode, IRQ14 and IRQ15 shall not be utilized by the SERIRQ stream nor mapped to other interrupt sources, and instead come from the GPIO controller. If the GPIO controller is entirely in ACPI mode, these interrupts can be mapped to other devices accordingly.



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Title	LPC,SPI,SMBUS,CLINK
Size	Document Number
Custom	Carlsberg_KL
Date	Wednesday, November 01, 2017
Sheet	18 of 106

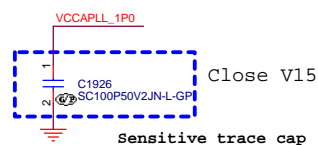
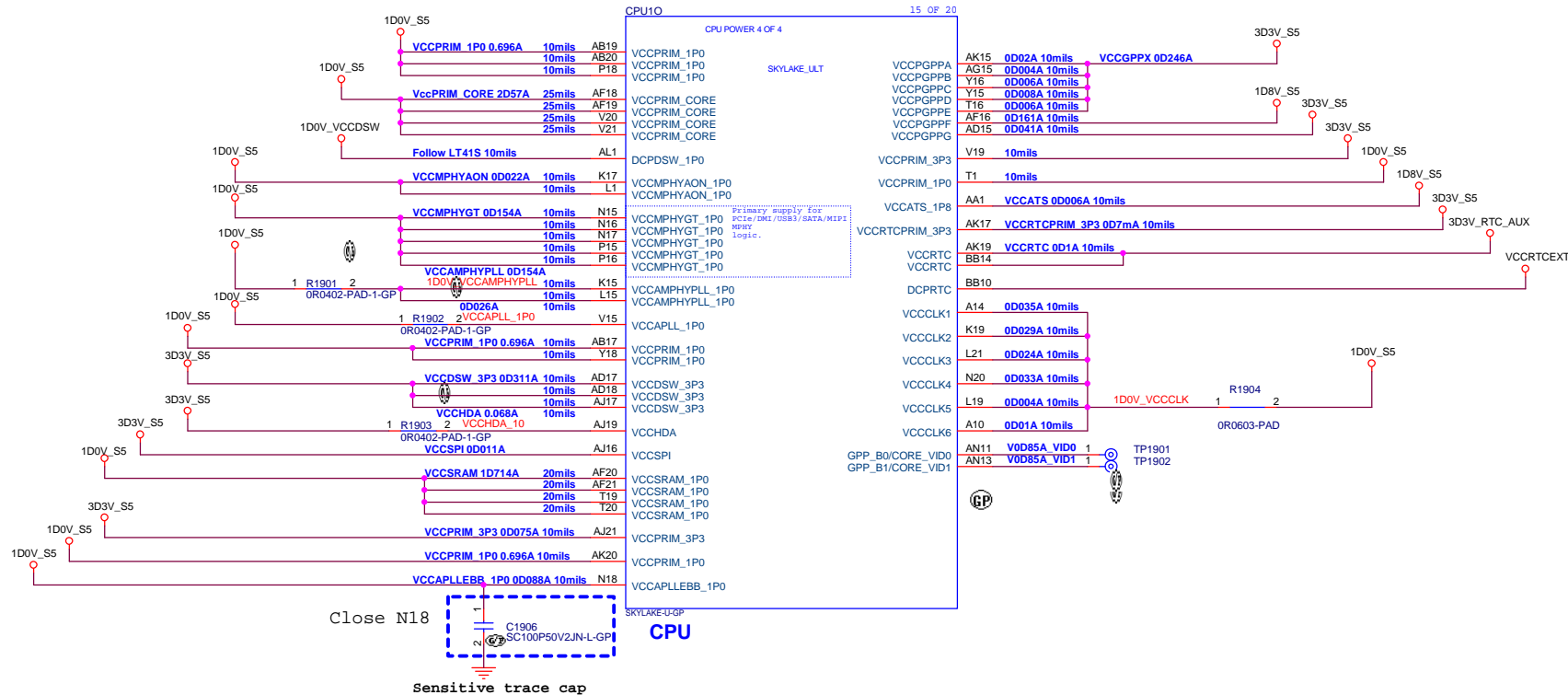


Table 2: eSPI/LPC Pinlist for SKL-PCH

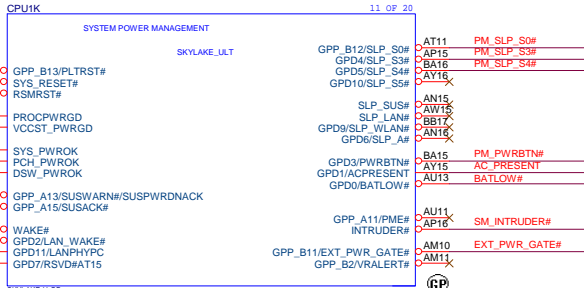
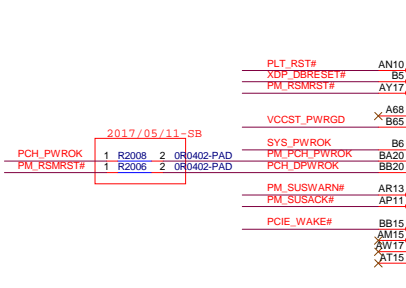
SKL-PCH Pin Name	Direction	LPC Signal	eSPI Signal	Pin Description
GPP_A_0	in	RCINB	<GPIO>	
GPP_A_1	inout	LAD_0	ESPI_IO_[0]	LPC Cmd/Addr/Data or eSPI Data [0]
GPP_A_2	inout	LAD_1	ESPI_IO_[1]	LPC Cmd/Addr/Data or eSPI Data [1]
GPP_A_3	inout	LAD_2	ESPI_IO_[2]	LPC Cmd/Addr/Data or eSPI Data [2]
GPP_A_4	inout	LAD_3	ESPI_IO_[3]	LPC Cmd/Addr/Data or eSPI Data [3]
GPP_A_5	out	LFRAMEB	ESPI_CSB	LPC Frame or eSPI Chip Select
GPP_A_6	inout	SERIRQ	<GPIO>	
GPP_A_7	iod	PIRQAB	<GPIO>	
GPP_A_9	out	LPC_CLKOUT_0	ESPI_CLK	
GPP_A_14	out	SUS_STATB	ESPI_RESETB	
GPP_C_5_SM L0ALERTB	input	ESPI_EN Pin Strap		eSPI Enable Pin Strap; sampled at RMSRST# deassertion 0: LPC; 1: eSPI
VCCPGPPA	-	3.3V	1.8V	Voltage for all GPIOs in GPP_A group

NOTE: All pin mappings are subject to change. Refer to the SKL-PCH EDS for final pin list.

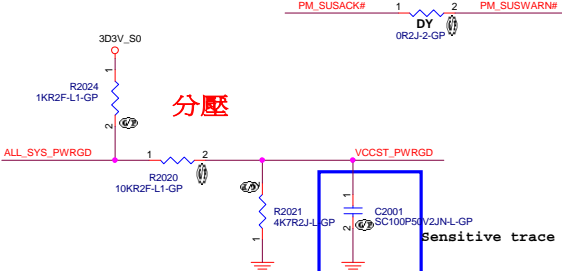
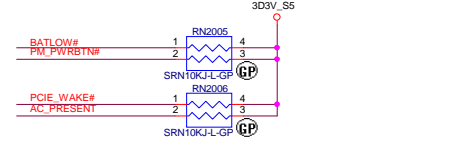
<Core Design>

Main Func = PCH

- 24 SYS_PWROK >>>
- 40 PCH_PWROK >>>
- 24,61,62,63 PCIE_WAKE# >>>
- 24,40 ALL_SYS_PWRGD >>>
- 24,61,62,63,68,89,91 PLT_RST# <<<
- 24 RSMRST#_KBC >>>
- 45,53,73 3V_5V_POK >>>
- 24,40 PM_SLP_S0# <<<
- 24,40,45,53 PM_SLP_S3# <<<
- 24,40,51 PM_SLP_S4# <<<
- 24 PM_PWRBTN# >>>
- 24 AC_PRESENT >>>



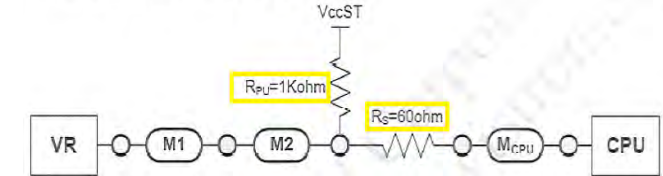
BATLOW#:
Pull-up required even if not implemented.



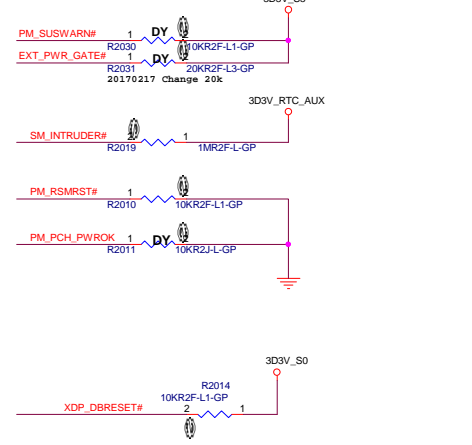
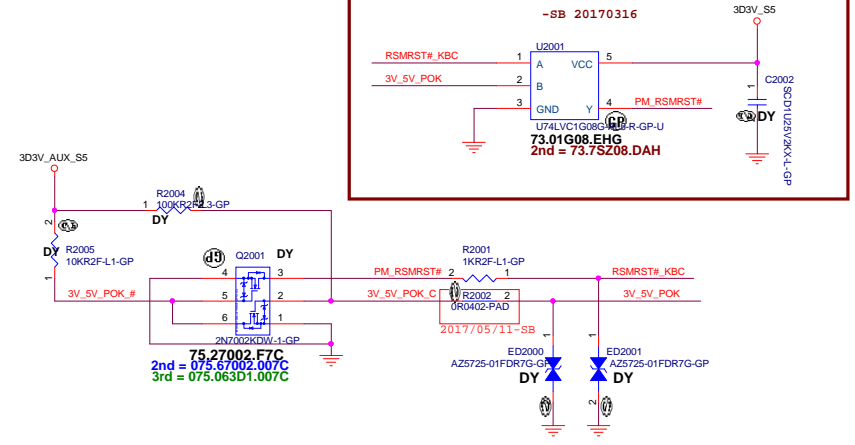
#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

VCCST_PWRGD / HWM201:

VCCST_PWRGOOD



VCCST_PWRGOOD is a signal on the processor that indicates both the VCCST power supply and VDDQ power supply are within voltage tolerance specification



GPP_A13-15 pin(LPC/eSPI):

Name	Internal Pull-Up/Pull-Down (Note 1)	De-Glitch (Note 2)		Multiplexed With	Default
		Input	Output		
GPP_A13	None	No	Yes	LPC mode: SUSWARN#/ SUSPWRDNACK eSPI mode: None	SUSWARN#/ SUSPWRDNACK (LPC mode) GPI (eSPI mode)
GPP_A14	None	No	Yes	LPC mode: SUS_STAT# eSPI mode: ESPI_RESET#	SUS_STAT# (LPC mode) ESPI_RESET# (eSPI mode)
GPP_A15	None	No	Yes	LPC mode: SUS_ACK# eSPI mode: None	SUS_ACK# (LPC mode) GPI (eSPI mode)

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File: CPU_(POWER MANAGEMENT)
Size: Custom
Document Number: Carlsberg_KL
Date: Wednesday, November 01, 2017
Sheet: 20 of 106
Rev: -1M

Main Func = PCH



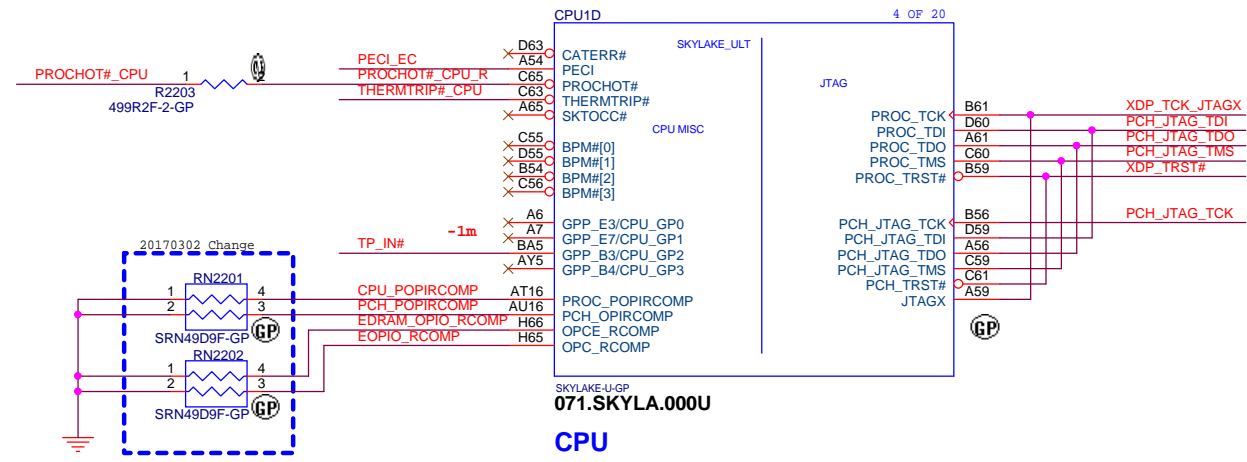
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Title CPU_(VSS)		
Size Custom	Document Number Carlsberg_KL	Rev -1M
Date: Wednesday, November 01, 2017 Sheet 21 of 106		

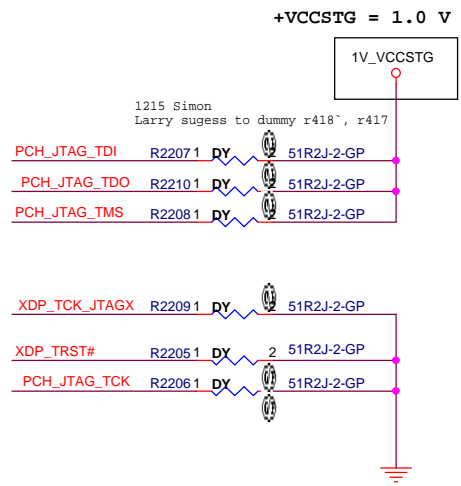
Main Func = CPU

24 PECL_EC <<>> _____
24,44,46 PROCHOT#_CPU <<>> _____

65 TP_IN# >>> _____



PROCHOT#	Processor Hot: PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GT L OD 0	SE	All processor lines
THERMTRIP#	Thermal Trip: The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin. Refer to the appropriate platform design guide for termination requirements.	0	OD	SE	All processor lines



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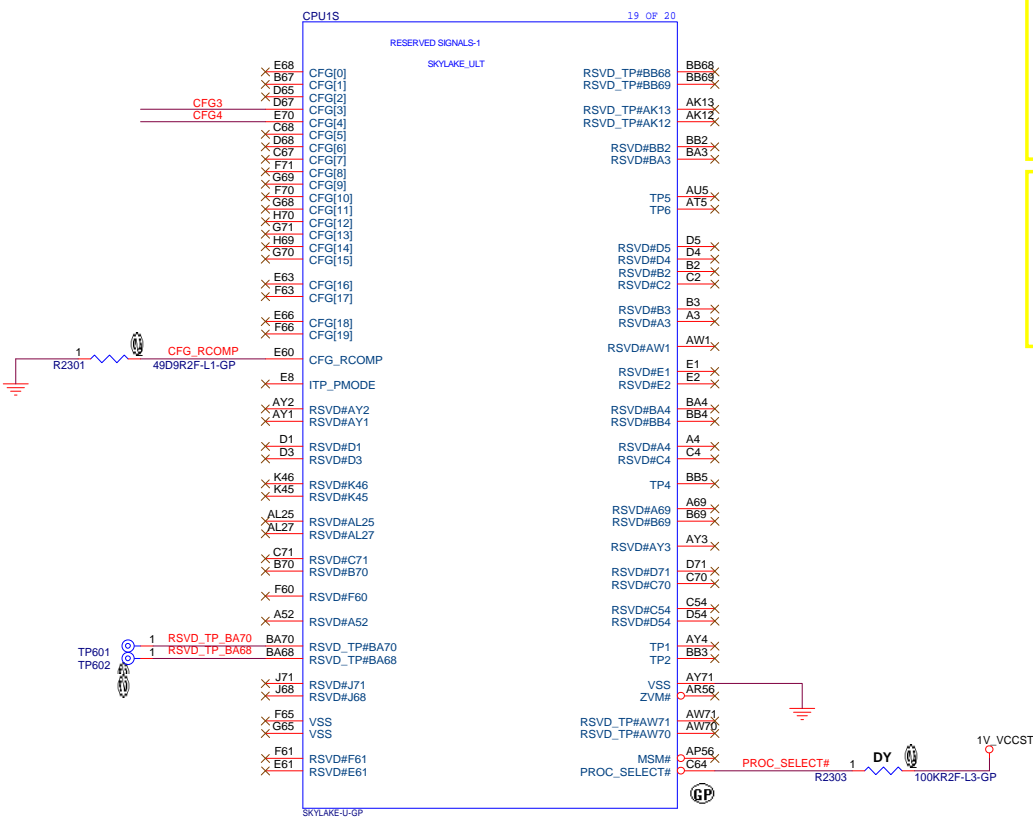
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Title **CPU_(JTAG/CPU SIDE BAND)**

Size Custom Document Number **Carlsberg_KL** Rev **-1M**

Date: Wednesday, November 01, 2017 Sheet 22 of 106

Main Func = CPU



CPU

CPU

PCH strap pin:

CFG3

R2305 1KR2J-1-GP

1 2

CFG3

[BDW Only] PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

PCH strap pin:

CFG4

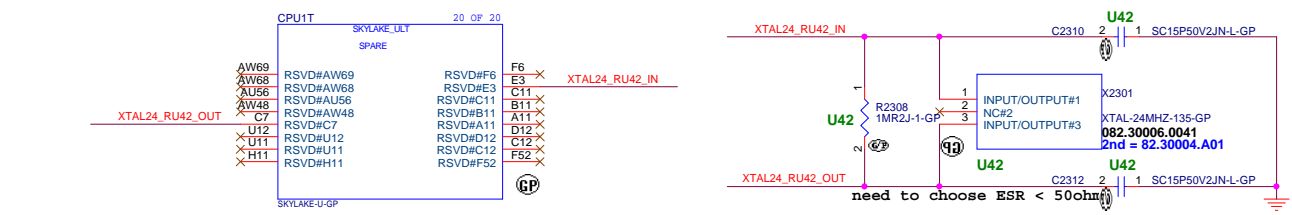
R2304 1KR2J-1-GP

1 2

CFG4

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port.
	1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none">• CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted:<ul style="list-style-type: none">– 1 = (Default) Normal Operation; No stall.– 0 = Stall.• CFG[1]: Reserved configuration lane.• CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.<ul style="list-style-type: none">– 1 = Normal operation– 0 = Lane numbers reversed.• CFG[3]: Reserved configuration lane.• CFG[4]: eDP enable:<ul style="list-style-type: none">– 1 = Disabled.– 0 = Enabled.• CFG[6:5]: PCI Express* Bifurcation<ul style="list-style-type: none">– 00 = 1 x8, 2 x4 PCI Express*– 01 = reserved– 10 = 2 x8 PCI Express*– 11 = 1 x16 PCI Express*• CFG[7]: PEG Training:<ul style="list-style-type: none">– 1 = (default) PEG Train immediately following RESET# de assertion.– 0 = PEG Wait for BIOS for training.• CFG[19:8]: Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.	
PROC_SELECT#	Processor Select: This pin is for compatibility with future platforms. It should be unconnected for SKL.				N/A	All processor lines



P/N: 082.30006.0041

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Title **CPU_RESERVED,CFG**

Size Custom Document Number **Carlsberg_KL** Rev **-1M**

Date: Wednesday, November 01, 2017 Sheet 23 of 106

SSID = KBC

Power

Signal

2017 05/22 -SB

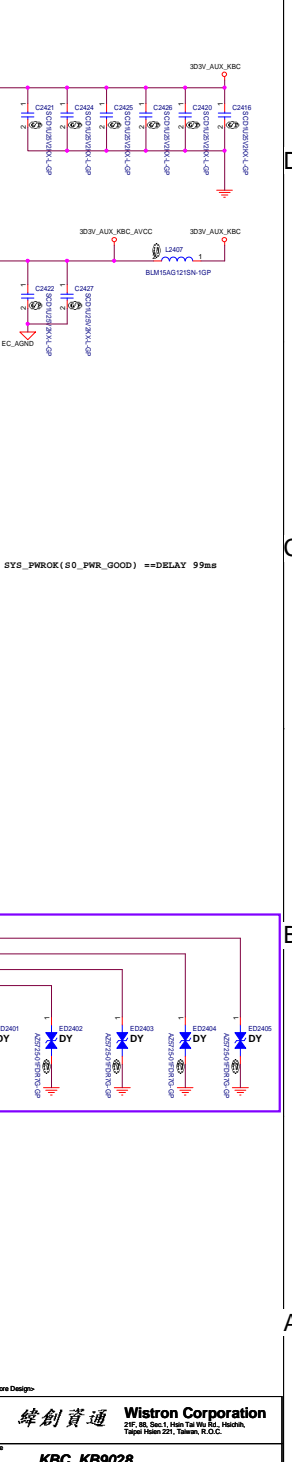
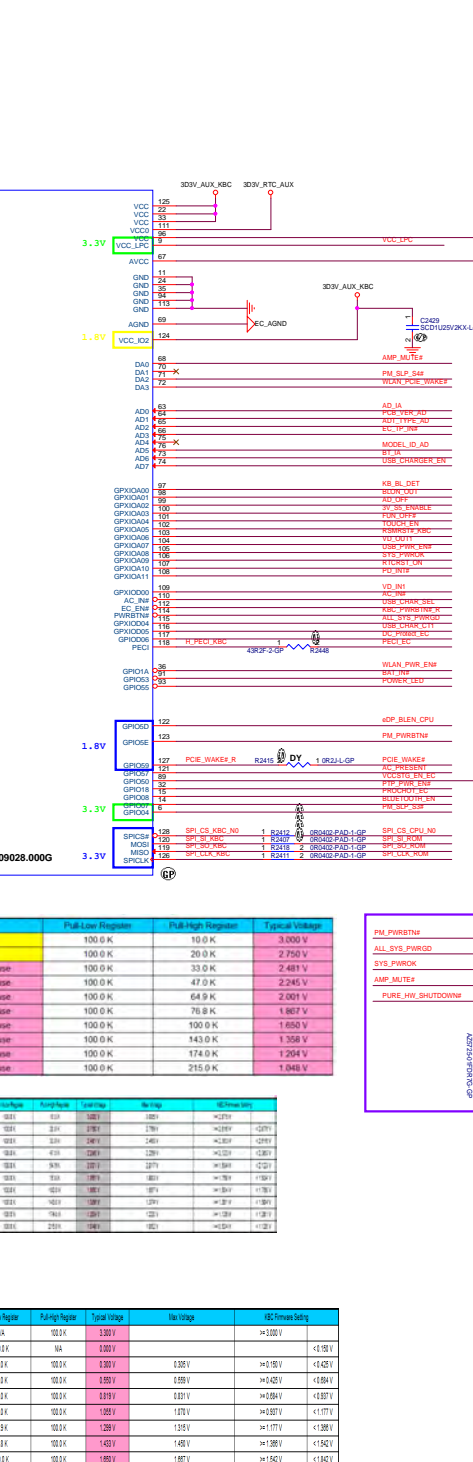
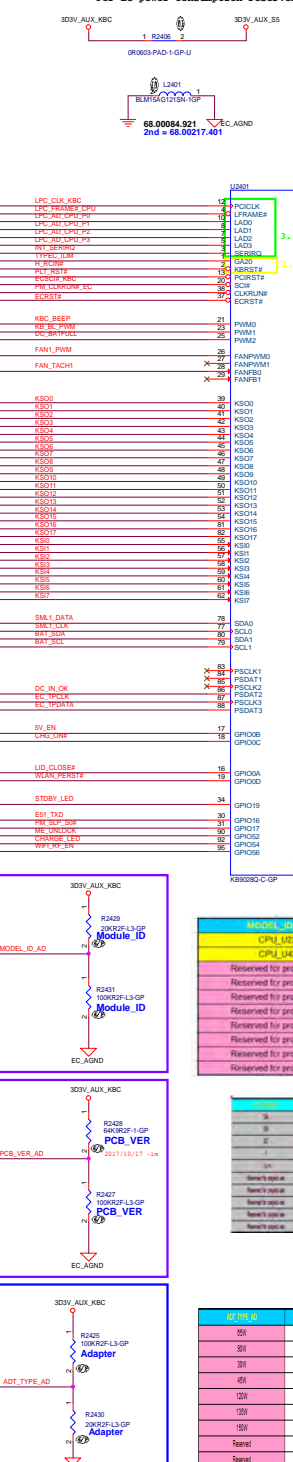
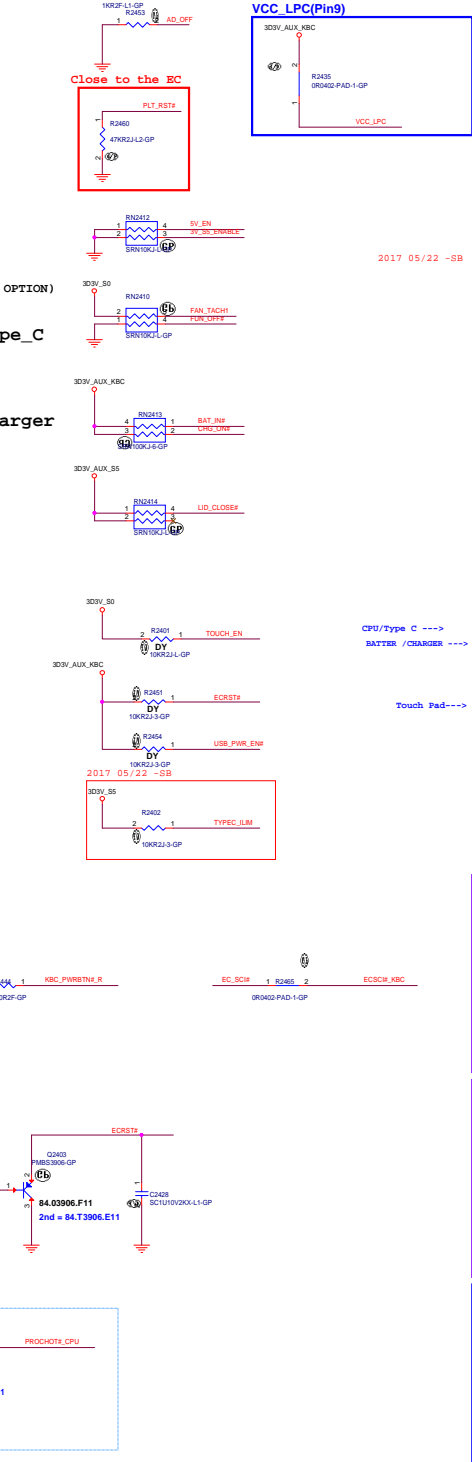
3.3V

LPC BUS=>3.3V
SPI BUS=>3.3V/1.8V (VCC_IO2 PIN:124 OPTION)

Type_C

Charger

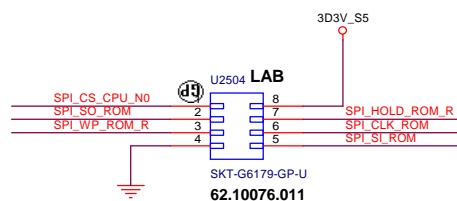
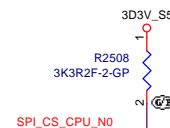
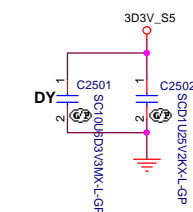
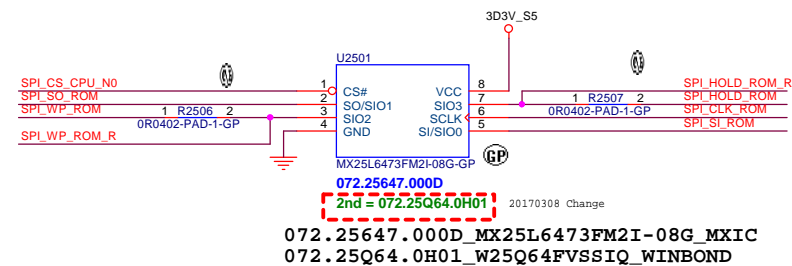
2017 05/22 -SB



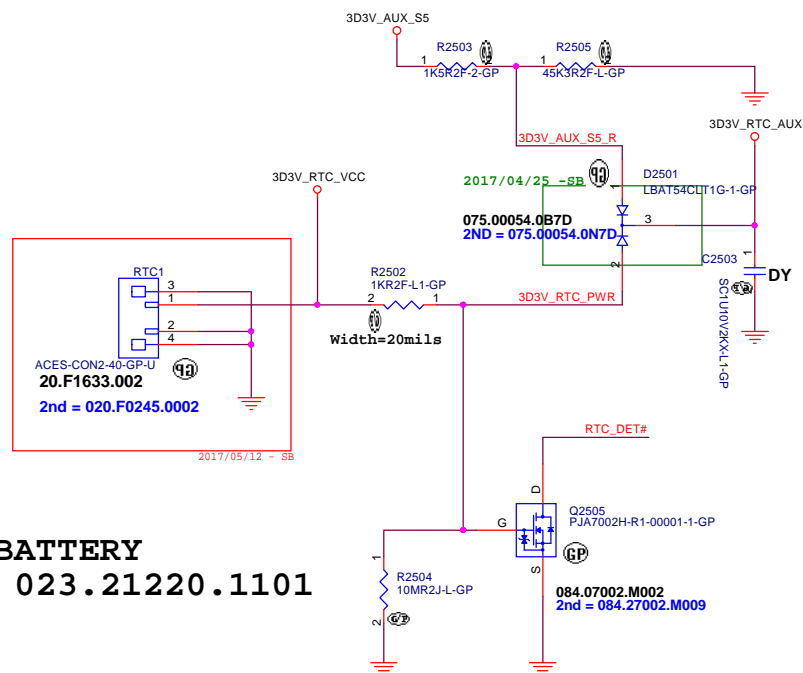
Main Func = SPI Flash

SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil



Main Func = RTC



RTC BATTERY

1st= 023.21220.1101

<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Flash(KBC+PCH)/RTC			
Size	Document Number	Rev	
Custom			
Carlsberg KL		-1M	
Date:	Wednesday, November 01, 2017	Sheet 25 of	106

24 VD_IN1 <<< _____

24,26,89 FAN1_PWM >>> _____

24,89 FAN_TACH1 <<< _____

24,40 PURE_HW_SHUTDOWN# <<< _____

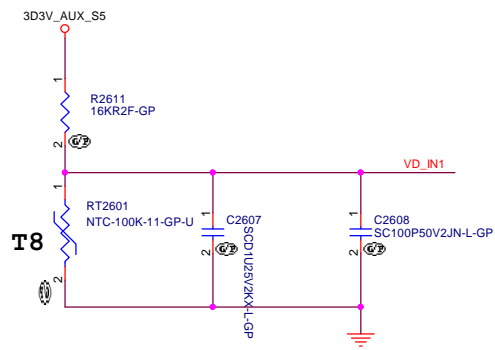
24 VD_OUT1 >>> _____

40,46 VR_RDY >>> _____

89 FAN_TACH1_C <<< _____

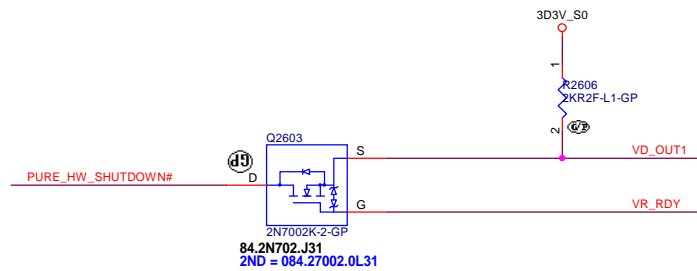
24,26,89 FAN1_PWM <<< _____

SSID = Thermal

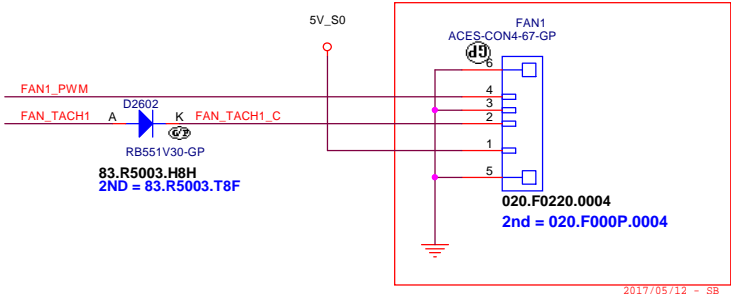
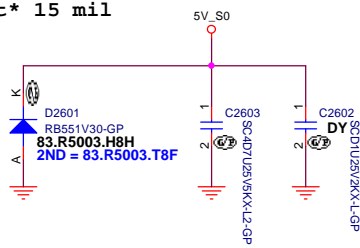


RT2601 close CPU and Vcore chock

VD_IN1 trace 10 mli



Layout 15 mil



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal 7718/Fan Controller P2793**

Size	Document Number	Rev
Custom	Carlsberg KL	-1M
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```

17  HDA_SDOUT_CODECD >>>_____
17  HDA_BITCLK_CODECD >>>_____
    17  HDA_SDIN3_CPU <<<_____
17  HDA_SYNC_CODECD >>>_____
17  HDA_RST#_CODECD >>>_____









```

17,55	DMIC_DATA_CON	»»	_____
17,55	DMIC_CLK_CON	»»	_____

29 AUD_SPK1_L+

29 AUD_SPK1_L-        

29 AUD_SPK1_R-

29 AUD_SPK1_R+        

```

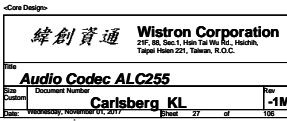
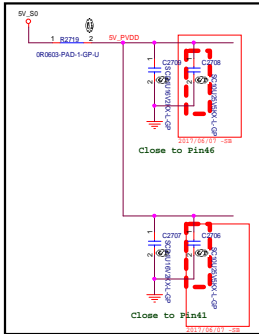
66,89      SELEEVE >>> _____
66,89      AUD_HP1_JACK_L2 <<< _____
66,89      AUD_HP1_JACK_R2 <<< _____
           66,89      RING2 >>> _____
           66,89      AUD_HP1_ID# >>> _____

```

```

24      AMP_MUTE# >>>_____
24      KBC_BEEP  >>>_____
14,17   HDA_SPKR  >>>_____

```



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<Core Design>

<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
AUDIO AMP ALC1001		
Size	Document Number	Rev
A3	Carlsberg_KL	-1M
Date:	Wednesday, November 01, 2017	Sheet 28 of 106

SSID = AUDIO

Speaker

2017/05/16 - SB

27 AUD_SPK1_L- <<<< —
27 AUD_SPK1_L+ <<<< —
27 AUD_SPK1_R- <<<< —
27 AUD_SPK1_R+ <<<< —

AUD_SPK1_L- R2914 1 2 0R0603-PAD
AUD_SPK1_L+ R2915 1 2 0R0603-PAD
AUD_SPK1_R- R2916 1 2 0R0603-PAD
AUD_SPK1_R+ R2917 1 2 0R0603-PAD

AUD_SPK1_L-_CON 1
AUD_SPK1_L+_CON 2
AUD_SPK1_R-_CON 3
AUD_SPK1_R+_CON 4

SPK1
ACES-CON4-17-GP-U1
20.F1621.004
2nd = 20.F1937.004

EC2901 1 2 SC22P50V2JN-L-GF DY
EC2902 1 2 SC22P50V2JN-L-GF DY
EC2915 1 2 SC22P50V2JN-L-GF DY
EC2920 1 2 SC22P50V2JN-L-GF DY

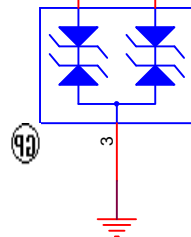
Layout Note:
Trace width=40mil

AFTP TESTPOINT

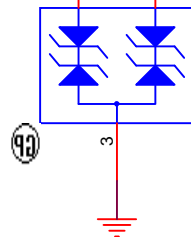
89 AUD_SPK1_L-_CON >>> —
89 AUD_SPK1_L+_CON >>> —
89 AUD_SPK1_R-_CON >>> —
89 AUD_SPK1_R+_CON >>> —

AUD_SPK1_L-_CON
AUD_SPK1_L+_CON

AUD_SPK1_R-_CON
AUD_SPK1_R+_CON



DY



DY

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緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Speaker/ALC255

Size
A4

Document Number

Carlsberg KL

Rev

-1M

Date: Wednesday, November 01, 2017

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

Carlsberg_KL

Rev
-1M

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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Carlsberg_KL</div>	Rev <div>-1M</div>
Date <div>Wednesday, November 01, 2017</div>		Sheet <div>31</div> of <div>106</div>

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<Core Design>

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number Carlsberg_KL		Rev -1M
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<Core Design>

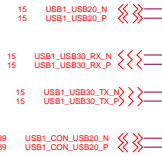
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Reserved			
Size A4	Document Number Carlsberg_KL		Rev -1M
Date: Wednesday, November 01, 2017		Sheet 33 of	106

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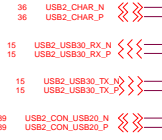
<Core Design>

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
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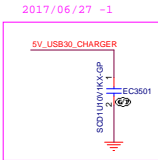
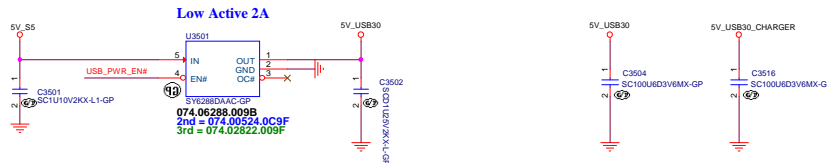
USB1



USB2

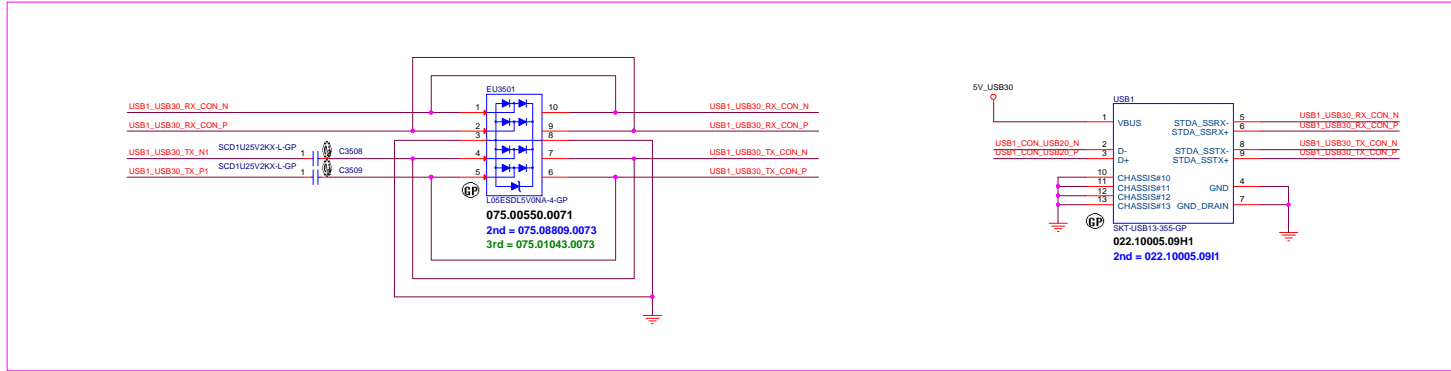


USB Power enable

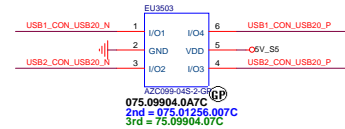
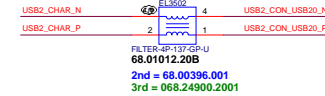


USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+ SuperSpeed RX
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+ SuperSpeed TX

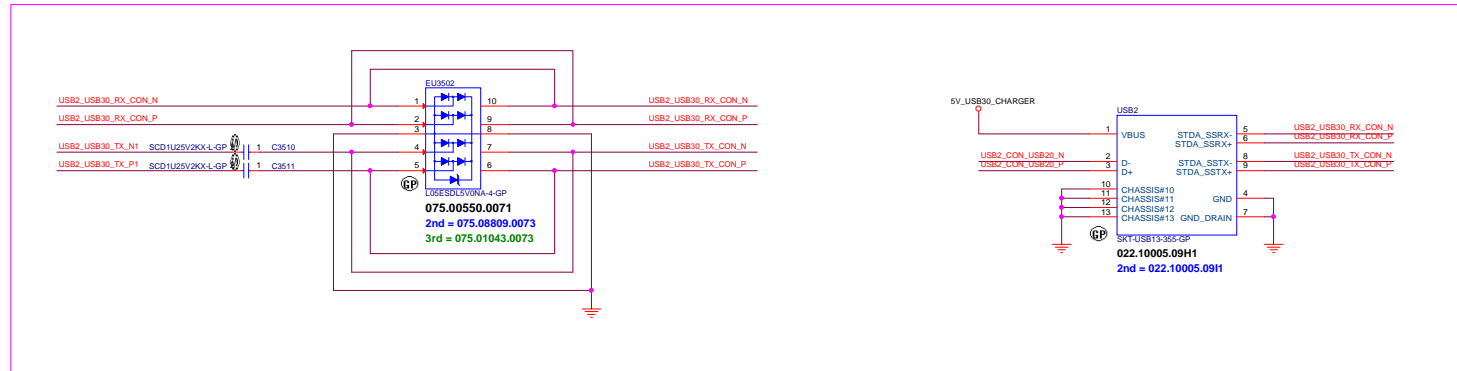
2017/06/29 -1



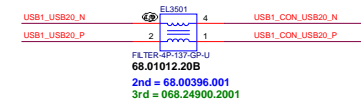
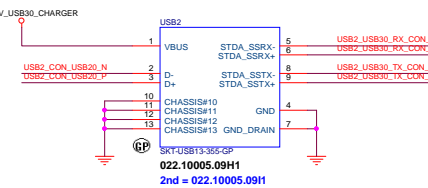
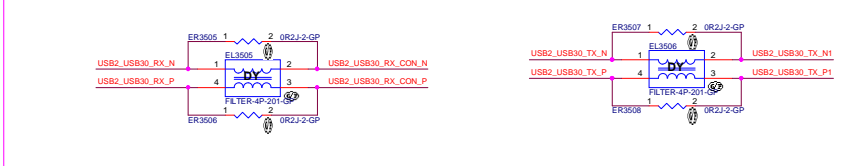
2017/06/29 -1



2017/06/29 -1



2017/06/29 -1



24 USB_CHARGER_EN >>>

24 USB_CHAR_SEL >>>

24 USB_CHAR_CT1 >>>

To Connector

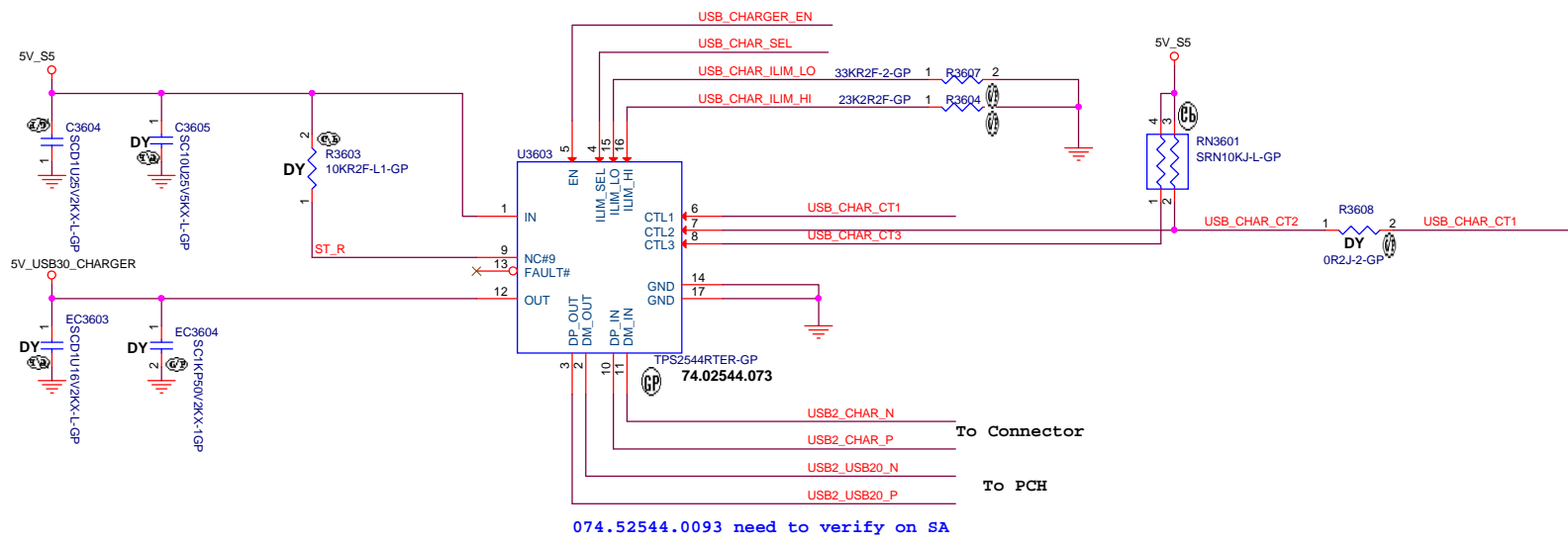
35 USB2_CHAR_N <<<

35 USB2_CHAR_P <<<

To PCH

15 USB2_USB20_N <<<

15 USB2_USB20_P <<<



CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	0	1	0	DCP_Auto	ILIM_HI	Data Lines Disconnected
0	1	1	X			
0	1	0	0	SDP1	ILIM_LO	Data Lines connected
0	1	0	1		ILIM_HI	
1	0	0	0	DCP Forced Shorted	ILIM_LO	Device Forced to stay in DCP BC 1.2 charging mode
1	0	0	1		ILIM_HI	
1	0	1	0	DCP / Divider1	ILIM_LO	Device Forced to stay in DCP Divider 1 Charging Mode
1	0	1	1		ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	
1	1	1	0	SDP2 ⁽¹⁾	ILIM_LO	Data Lines Connected
1	1	1	1	CDP ⁽¹⁾	ILIM_HI	

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Title: **USB CHARGER**

Size: Custom Document Number: **Carlsberg KL** Rev: **-1M**

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Title Reserved			
Size A4	Document Number Carlsberg_KL		Rev -1M
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Title USB RE_DRIVER_3D CAMERA			
Size A3	Document Number Carlsberg KL		Rev -1M
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<Core Design>

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Title Reserved			
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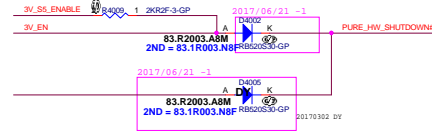
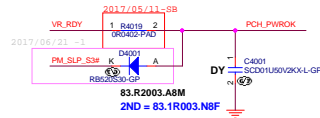
Power Sequence

26,46	VR_RDY	>>>
20	PCH_PWROK	<<<
20,24	PM_SLP_S0#	>>>
20,24,40,45,53	PM_SLP_S3#	>>>
24	3V_SL_ENABLE	>>>
45	3V_EN	<<<
24,45	5V_EN	<<<
24,26	PURE_HW_SHUTDOWN#	>>>
20,24	ALL_SYS_PWRGD	<<<
46	VCORE_EN	<<<
51	PWR_VDDQ_PG	>>>

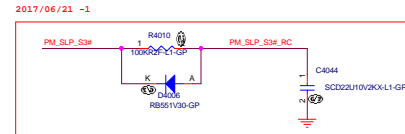
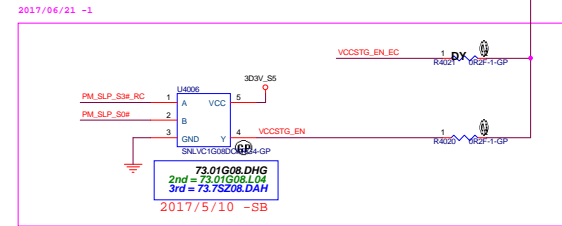
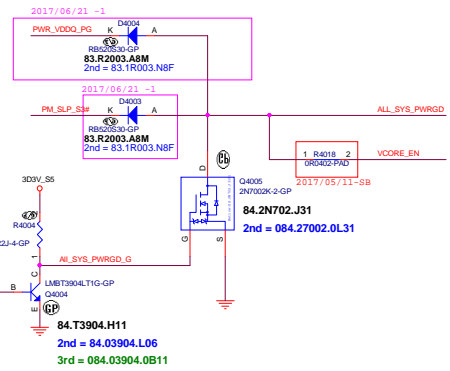
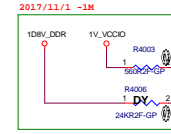
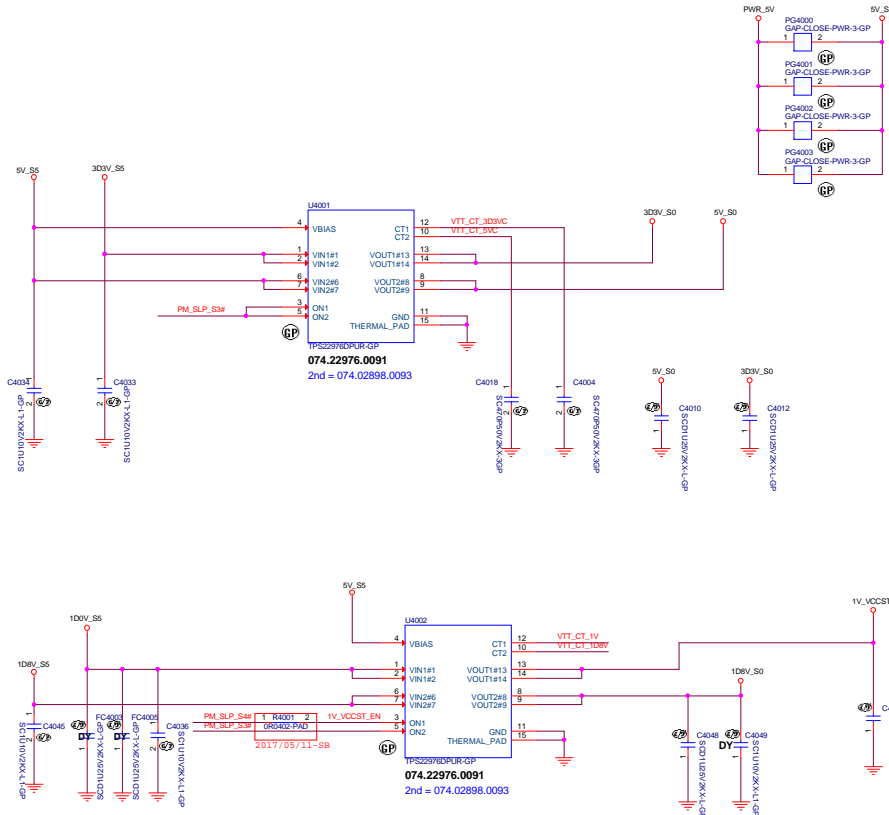
Run Power

20,24,51	PM_SLP_S0#	>>>
20,24,40,45,53	PM_SLP_S3#	>>>
24	VCCSTG_EN_EC	>>>

Power Sequence



ANNIE Run Power



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File	Power Plane Enable & SEQUENCE
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-1M

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

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Size
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-1M

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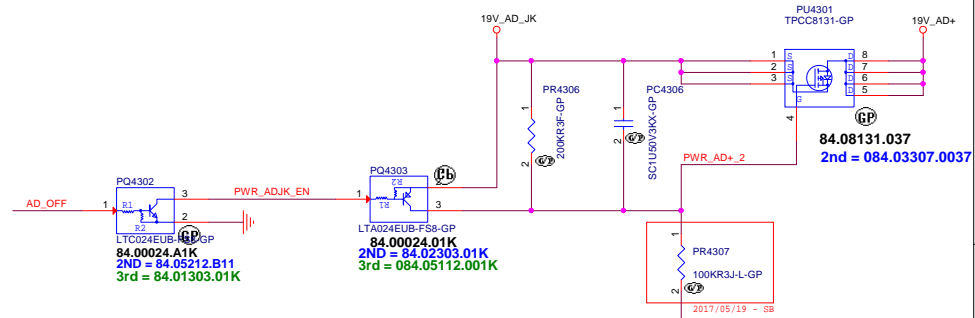
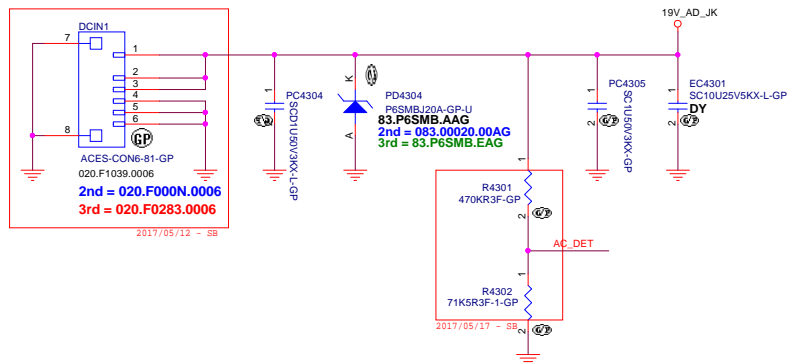
DC IN

24,44 BAT_IN# <<<
24,44 BAT_SCL <<<
24,44 BAT_SDA <<<

24 AD_OFF >>>
74 AC_DET <<<

24,65,89 KBC_PWRBTN# <<<

Adaptor in to generate DCBATOUT

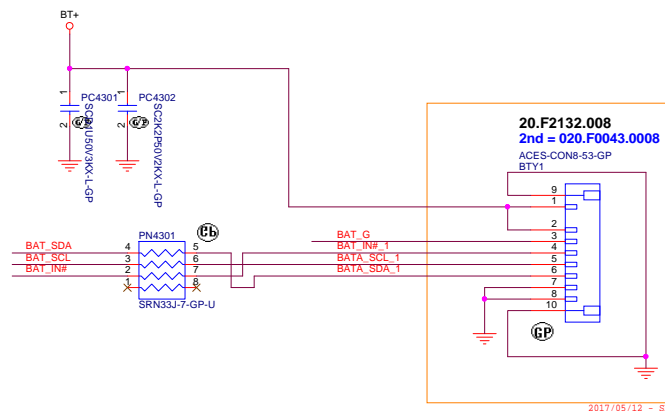


AFTP

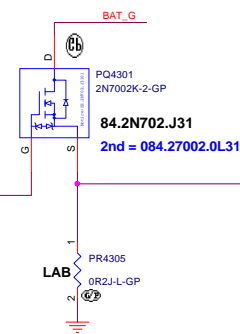
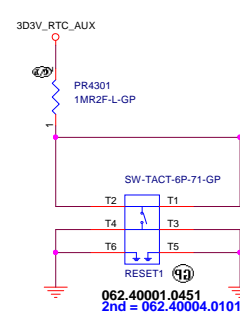
89 BAT_G <<<
89 BAT_IN#_1 <<<
89 BATA_SCL_1 <<<
89 BATA_SDA_1 <<<

Power Button

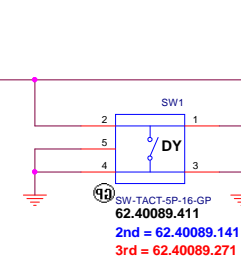
BATTERY CONNECTOR



Battery Reset

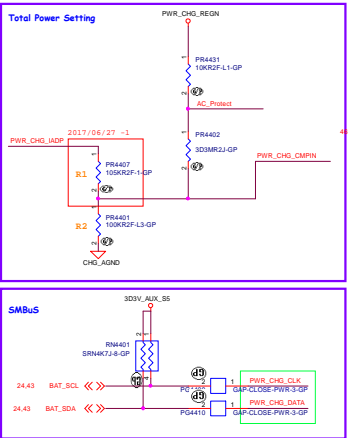


Battery Insert

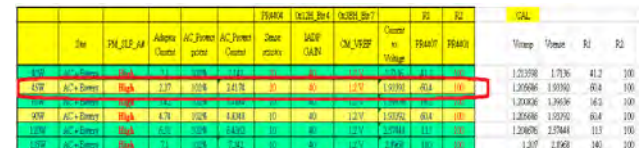


<Core Design>

45 PWR_CHG_ILIM <<<—



```
45 Watt AC Protect 110% , PR4407 change 73.2K ohm. ( 64.73225.6DL)
65 Watt AC Protect 110% , PR4407 change 150K ohm. ( 64.15035.6DL)
```



Wistron Corporation
21F, 88, Sec. 1, Hsiao Tai Wu Rd., Hsichih

File	Document Number
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Custom **Carlsberg KL**

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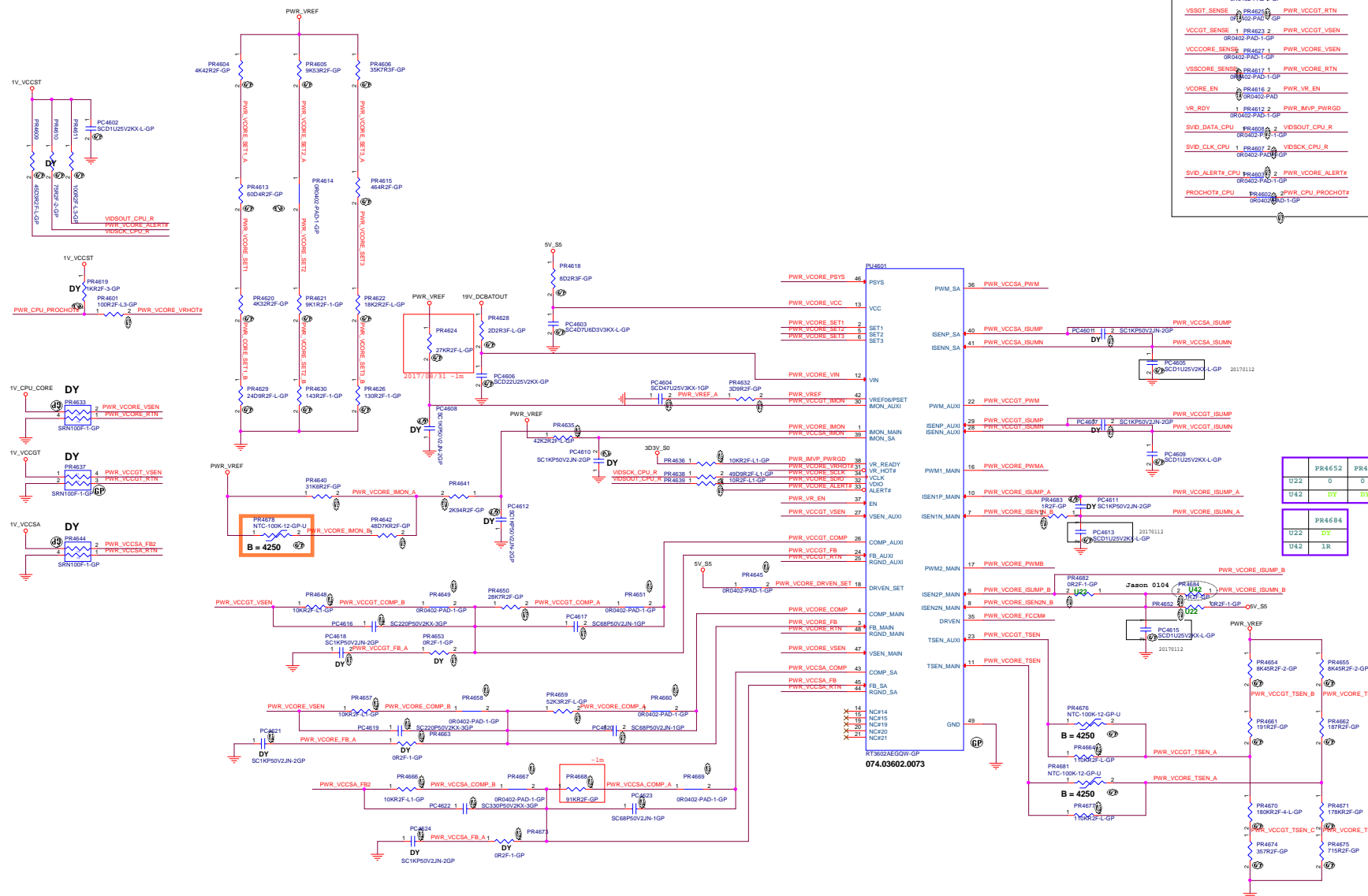
	PROCHOT*_CPU	<<<	_____
7	SVID_ALERT*_CPU	<<<	_____
7	SVID_CLK_CPU	>>>	_____
7	SVID_DATA_CPU	>>>	_____
26,40	VR_RDY	<<<	_____
40	VCORE_EN	>>>	_____
7	VSSCORE_SENSE	>>>	_____
7	VCCCORE_SENSE	>>>	_____
8	VCCGT_SENSE	>>>	_____
8	VSSGT_SENSE	>>>	_____
8	VSSSA_SENSE	>>>	_____
8	VCCSA_SENSE	>>>	_____
44	PSYS	>>>	_____

```

50 PWR_VCCSA_ISUMP >>>
PWR_VCCSA_ISUMN >>>
48 PWR_VCCGT_ISUMP >>>
48 PWR_VCCGT_ISUMN >>>
PWR_VCORE_ISUMP_A >>>
PWR_VCORE_ISUMN_A >>>
PWR_VCORE_ISUMP_B >>>
PWR_VCORE_ISUMN_B >>>

50 PWR_VCCSA_PWM <<<
PWR_VCCGT_PWM <<<
48 PWR_VCORE_PWMMA <<<
48 PWR_VCORE_PWMNB <<<
48 PWR_VCORE_PWMNB <<<
50 PWR_VCORE_FCCM <<<

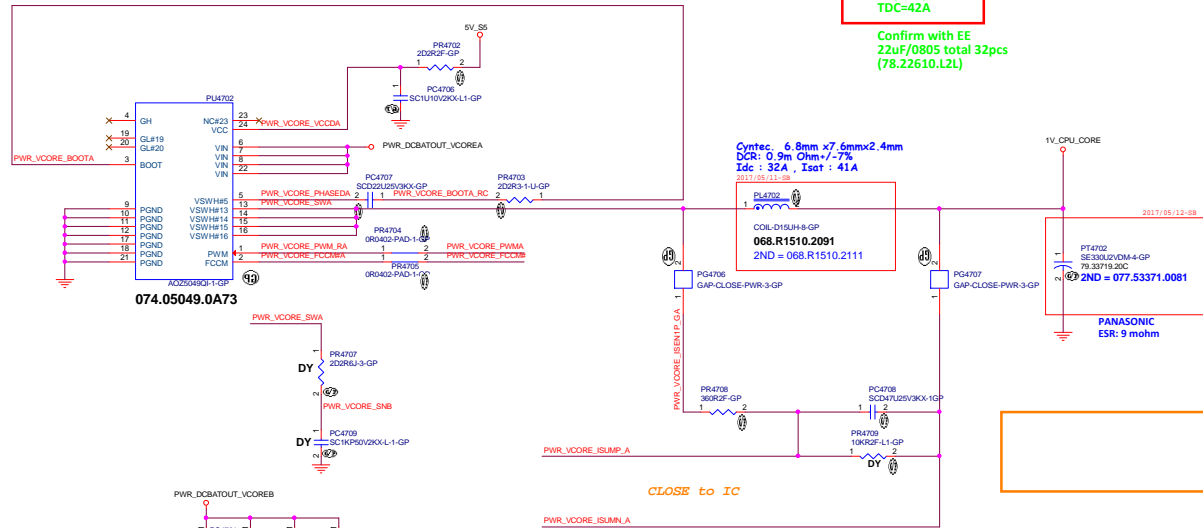
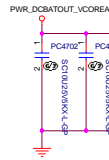
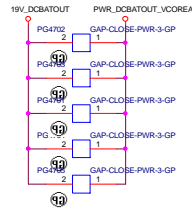
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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title		CPU_VCORE(1/3)	
Size	Document Number		Rev
Customer	Carlsberg KL		-1
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46	PWR_VCORE_SUMP_A	<<<	_____
46	PWR_VCORE_SUMP_LA	<<<	_____
46	PWR_VCORE_PWMA	>>>	_____
46,48,50	PWR_VCORE_FOCM#	>>>	_____
46	PWR_VCORE_ISUMP_B	<<<	_____
46	PWR_VCORE_ISUMP_LB	<<<	_____
46	PWR_VCORE_PWMB	>>>	_____



Confirm with EE
22uF/0805 total 32pcs
(78.22610.L2L)

Cyntec: 6.8mm x7.6mmx2.4mm
DCR: 0.9m Ohm+/-7%
Idc : 32A , Isat : 41A
2017/05/11-SB

PL4702

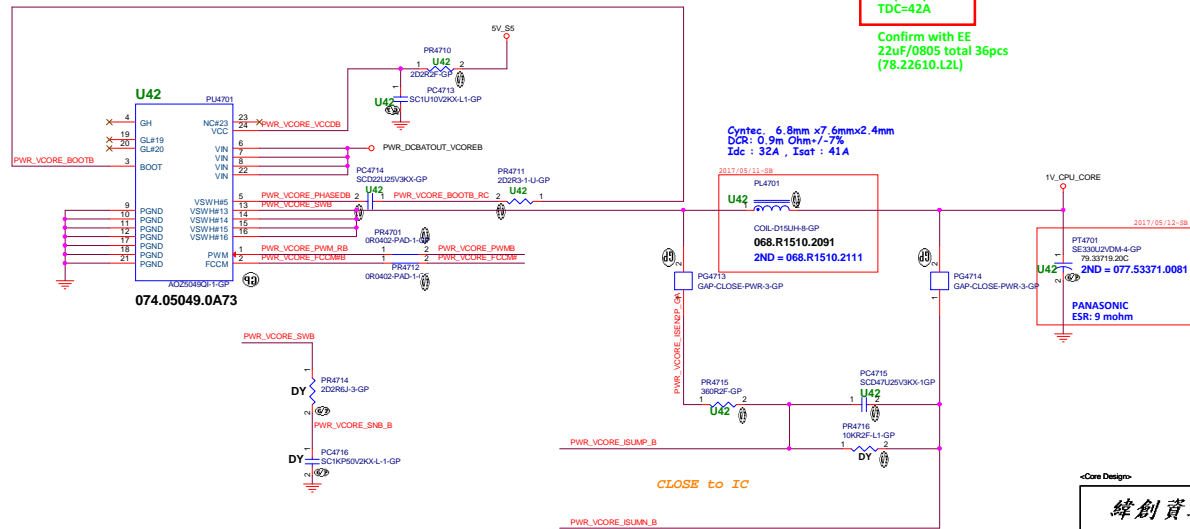
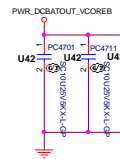
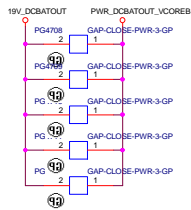
COIL-D15UH+8-GP
068.R1510.2091
2ND = 068.R1510.2111

2017/05/12-SB

54-GP

7.53371.0081

SONIC
mohm



Confirm with EE
22uF/0805 total 36pcs
(78.22610.L2L)

Cyntec. 6.8mm x7.6mmx2.4mm
DCR: 0.9m Ohm+/-7%
Idc : 32A , Isat : 41A

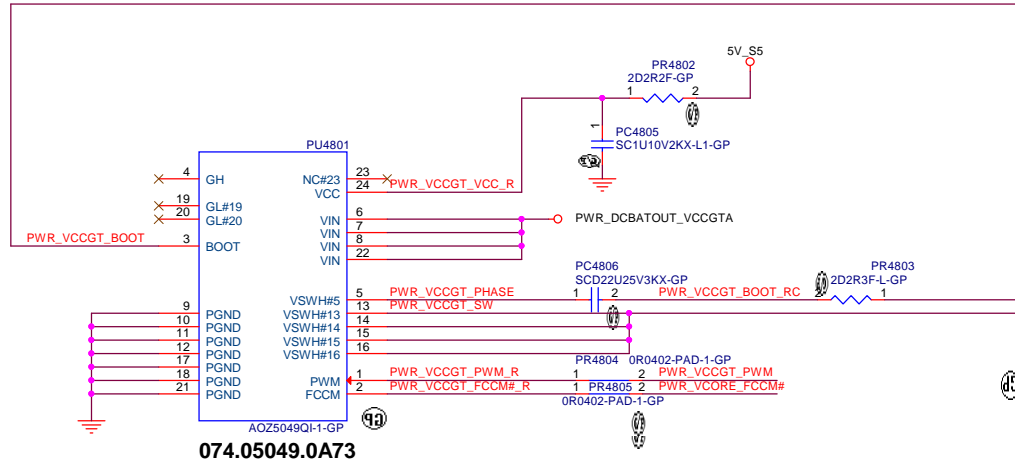
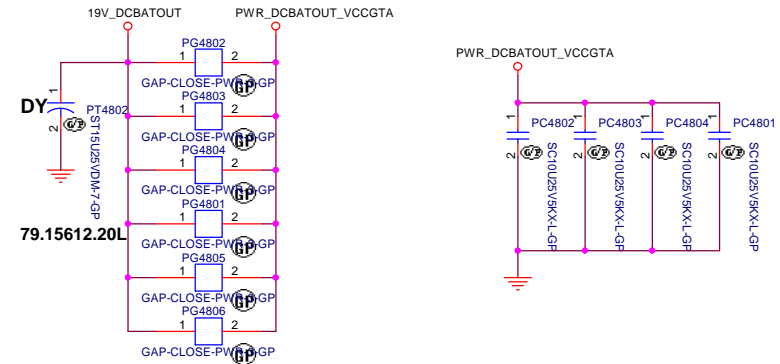
2017/05/12-SB

PT4701
SE330U2VDM-4-GP
79.33719.20C
2ND = 077.53371.0081

PANASONIC
ESR: 9 mohm

Main Func = CPU_CORE

46 PWR_VCCGT_ISUMP <<< _____
46 PWR_VCCGT_ISUMN <<< _____
46 PWR_VCCGT_PWM >>> _____
46,47,50 PWR_VCORE_FCCM# >>> _____



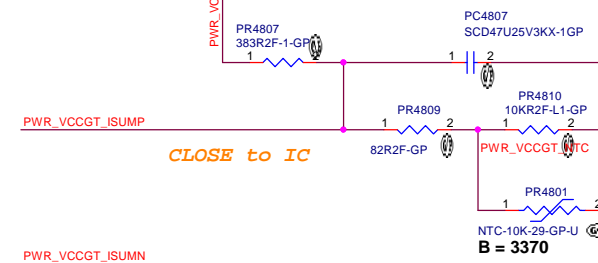
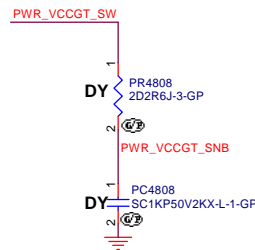
Cyntec. 6.8mm x7.6mmx2.4mm
DCR: 0.9m Ohm+/-7%
Idc : 32A , Isat : 41A

SKL_U42
Icc(max)=28A
TDC=12A

Confirm with EE
22uF/0805 total 26pcs
(78.22610.L2L)

2017/05/11-SB
PL4801
COIL-D15UH-8-GP
068.R1510.2091
2ND = 068.R1510.2111

2017/05/12-SB
PT4801
SE330U2VDM-4-GP
33719.20C
2ND = 077.53371.0081



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title			CPU VCCGT(3/3)	
Size	Document Number	Rev		-1M
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<Core Design>

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Title

Reserved

Size
A4

Document Number

Carlsberg_KL

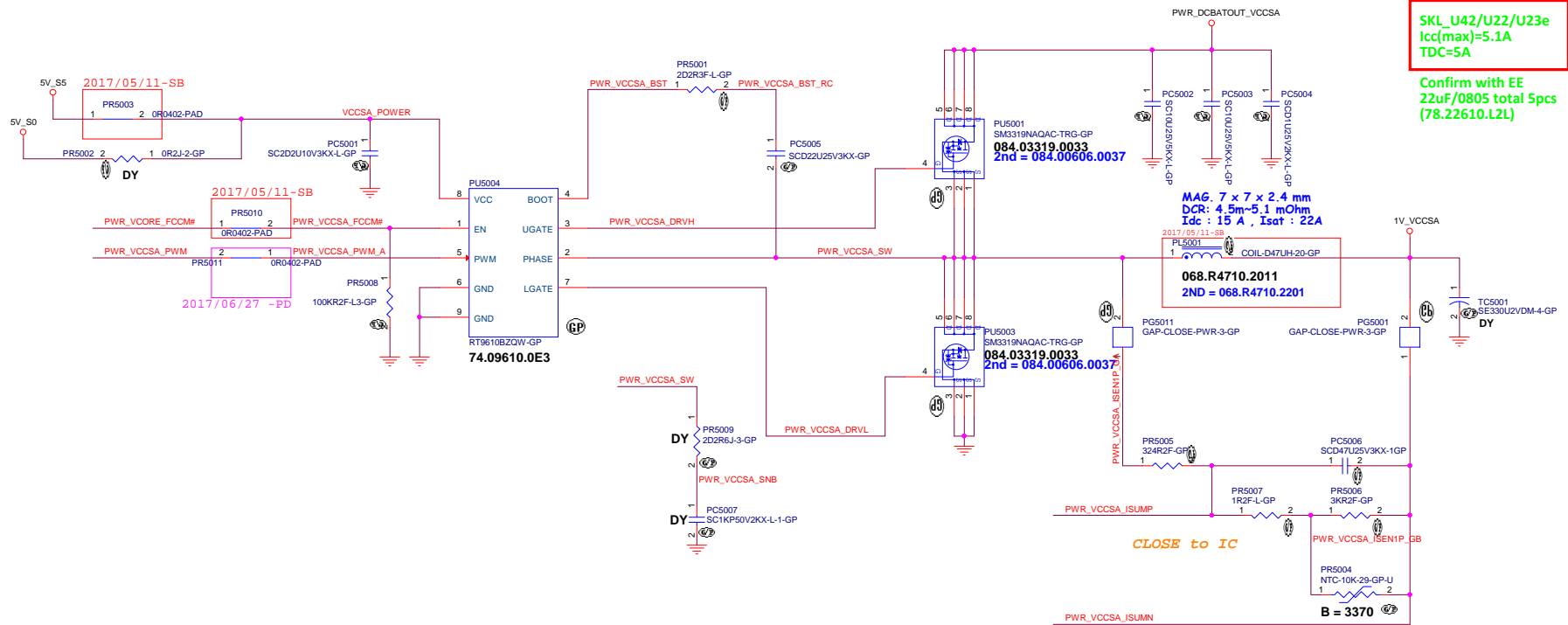
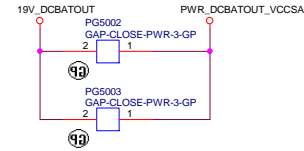
Rev

-1M

Date: Wednesday, November 01, 2017

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```
Main Func = CPU_CORE
```



<Core Design>

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Title

VCCSA

Size

Document Number

Carlsberg_KL

rev

-1M

Date:

Wednesday, November 14, 2018

9 KL
Sheet

50

100

TIME

53 1D8V_S5_PWRGD

PR5108 = 510K
Fs = 400-550KHz

TDC : 3.5A

MAG 7 x 7 x 2.4 mm
DCR: 11.2m~13.5mOhm
Idc : 9 A , Isat : 16A

2ND = 068.1R010.2351

$V_{out} = 0.75 \cdot (1 + R1/R2) = 1.0V$

074.05388.0043

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

G5388K 1D0V

Size

Document Number

A3

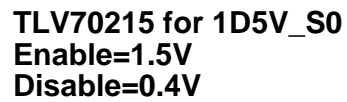
Carlsberg KL

Rev

-1M

Date: Wednesday, November 01, 2017

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<Core Design>

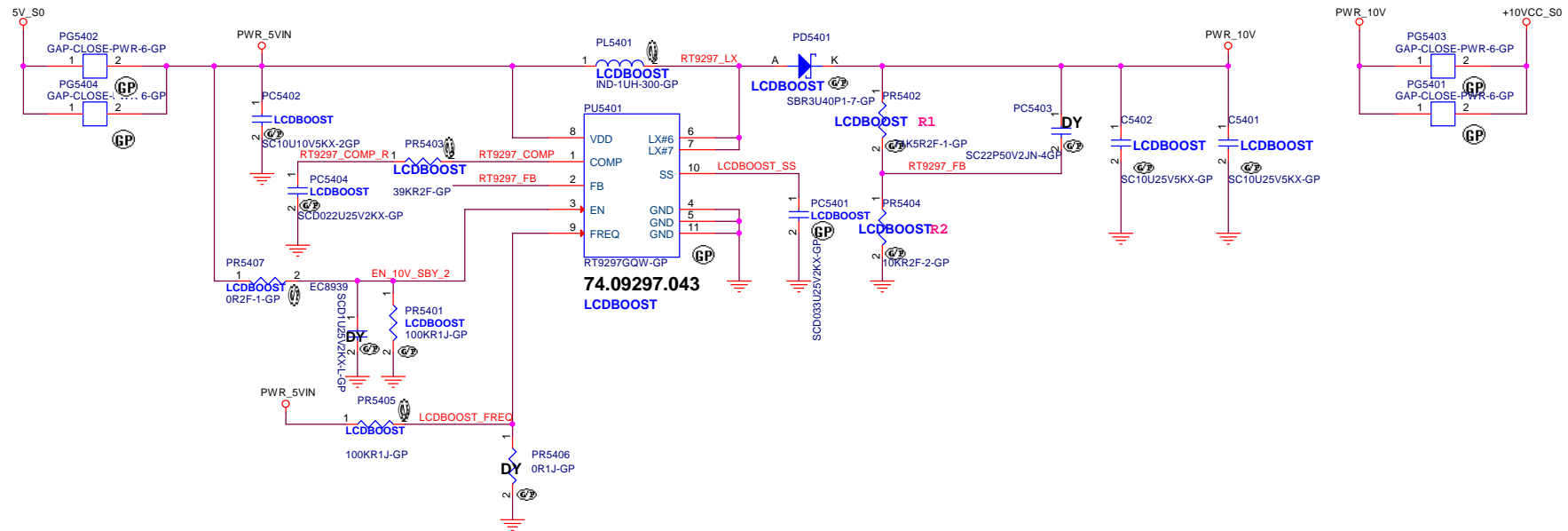
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title				RT8068_1D8V			
Size	Document Number						Rev
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2017/05/12 - SB new add

Cyntec 1.0uH 2520 Size
Idc=3.0A, Isat=4.0A

+10VCC , I_{max}= 1.5A

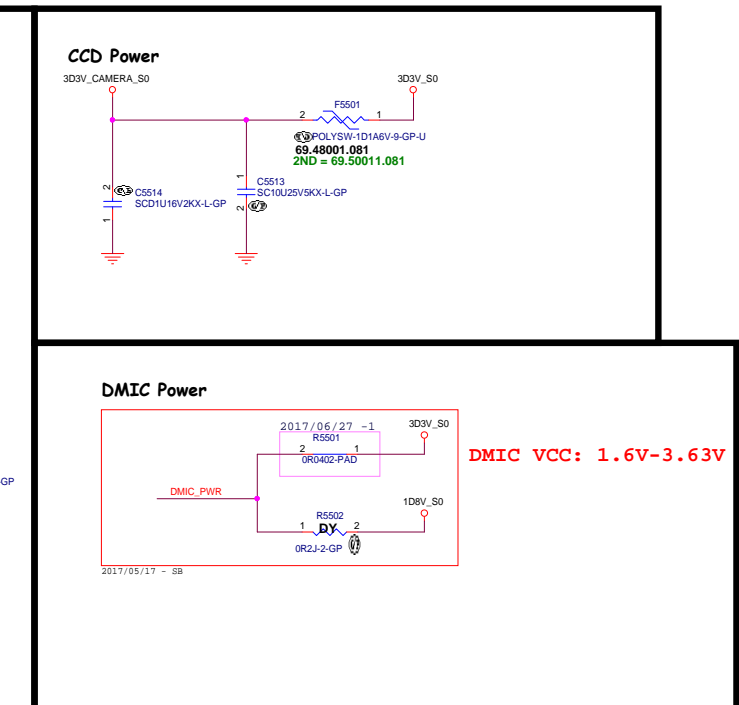
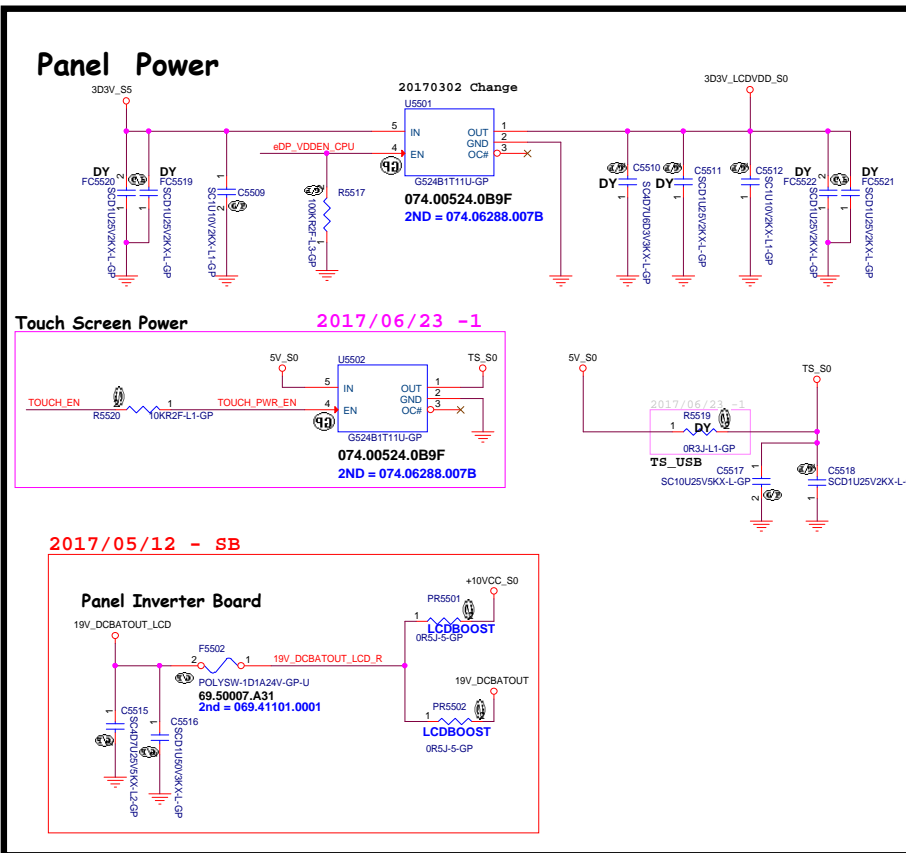
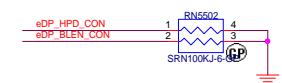
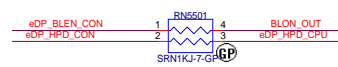
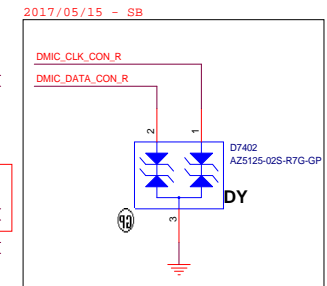
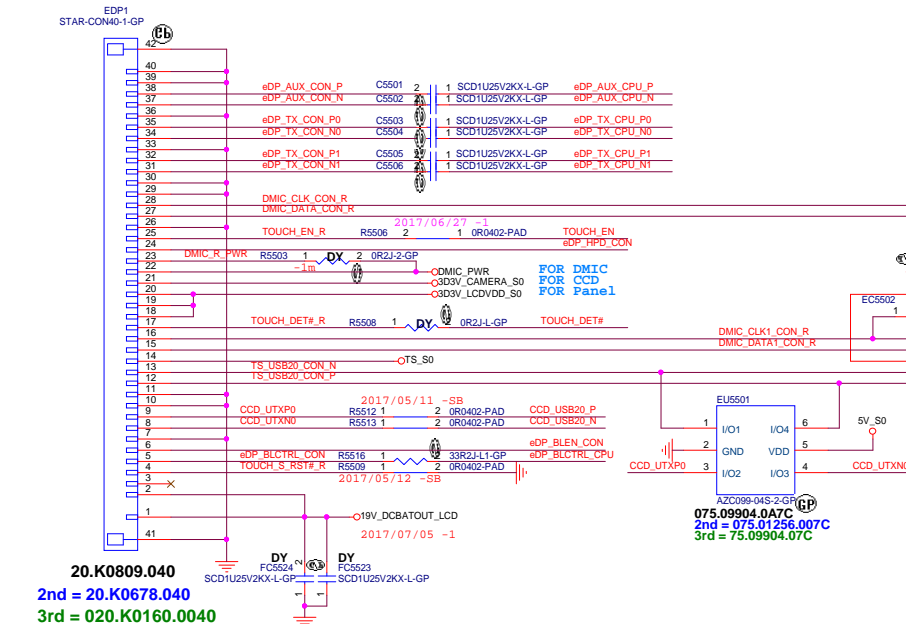


Control Inputs						
EN, FREQ Input Low Voltage	V_{IL}		--	--	$0.3 \times V_{DD}$	V
EN, FREQ Input High Voltage	V_{IH}		$0.7 \times V_{DD}$	--	--	V
EN, FREQ Input Hysteresis			--	$0.1 \times V_{DD}$	--	V
FREQ Pull-down Current			--	6	--	μA
EN Input Current	I_{EN}	EN = GND	--	0.001	1	μA

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Title				LCD Backlight Boost			
Size A3	Document Number					Rev	
	Carlsberg_KL					-1M	
Date:	Wednesday, November 01, 2017			Sheet	54	of	106



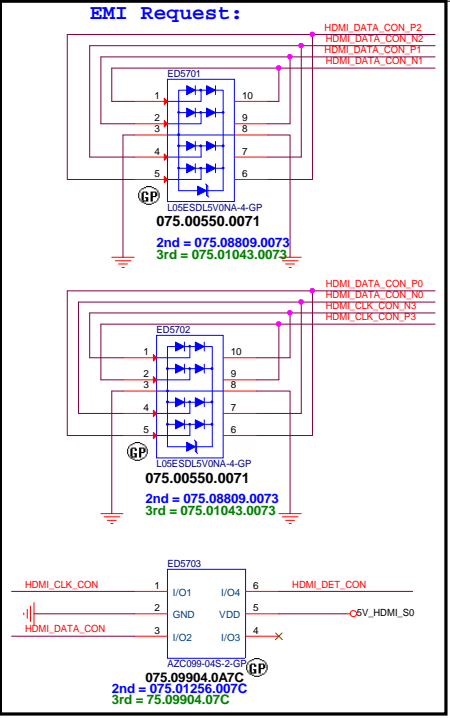
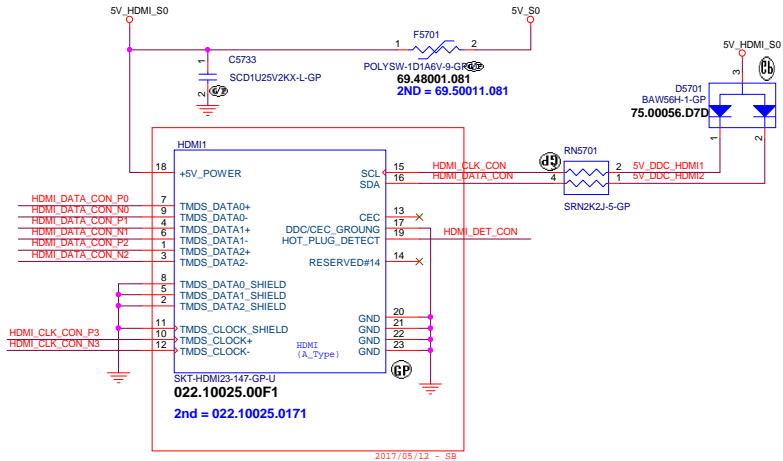
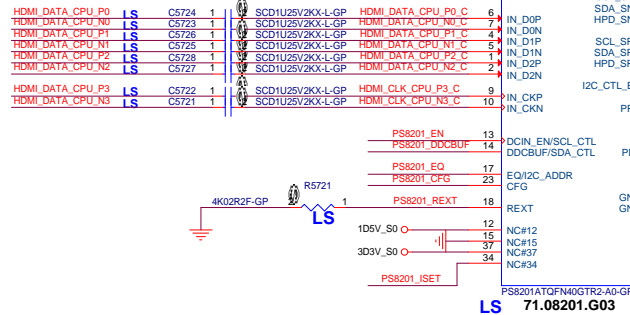
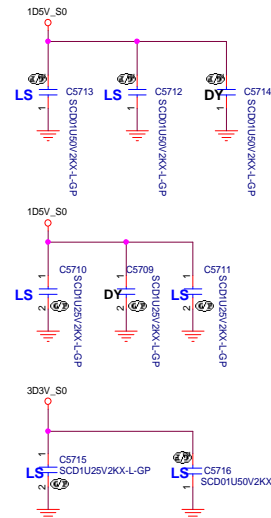
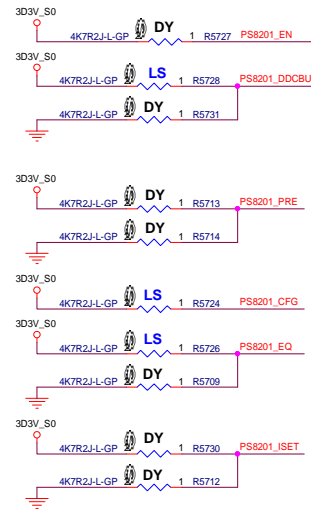
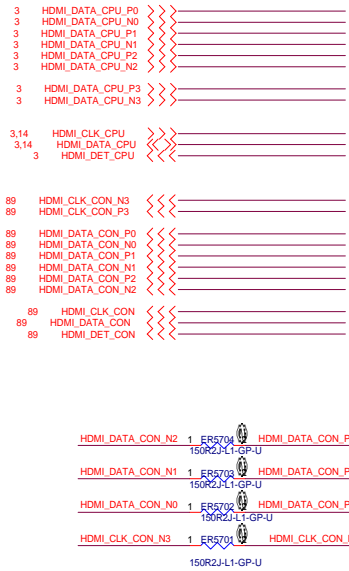
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
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SSID = VIDEO

HDMI Level Shifter & CONNECTOR



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緯創資通

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Title

Reserved

Size
A

Document Number

Carlsberg_KL

Rev

-1M

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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>DVI(Reserved)</div>		
Size <div>A4</div>	Document Number <div>Carlsberg_KL</div>	Rev <div>-1M</div>
Date: Wednesday, November 01, 2017		Sheet 59 of 106

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Title

HDD GSENSOR

Size
Custom

Document Number

Carlsberg_KL

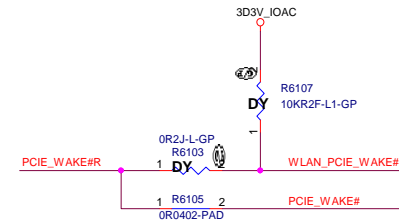
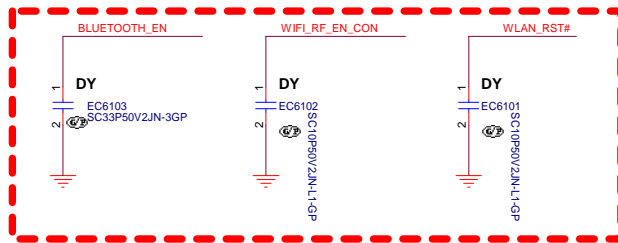
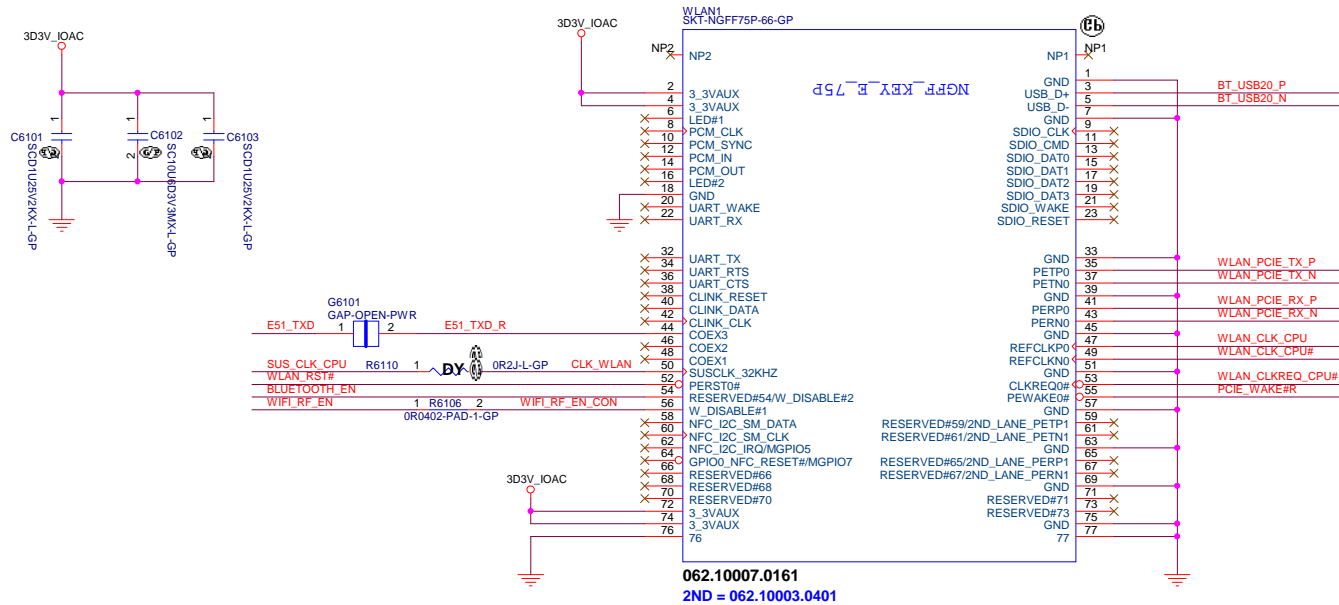
Rev
-1M

Date: Wednesday, November 01, 2017

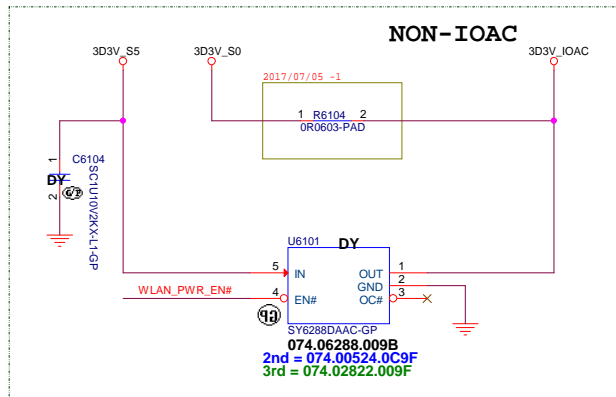
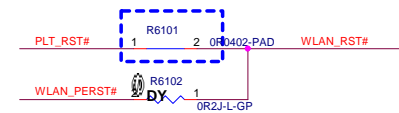
Sheet 60 of 106

SSID = Wireless Mini Card Connector(802.11a/b/g/n)

24,68	E51_TXD	>>>	_____
24,89	BLUETOOTH_EN	>>>	_____
24	WIFI_RF_EN	<<<	_____
20,24,62,63,68,89,91	PLT_RST#	>>>	_____
24	WLAN_PERST#	>>>	_____
15,89	WLAN_PCIE_TX_P	>>>	_____
15,89	WLAN_PCIE_TX_N	>>>	_____
15,89	WLAN_PCIE_RX_P	<<<	_____
15,89	WLAN_PCIE_RX_N	<<<	_____
16,89	WLAN_CLK_CPU	>>>	_____
16,89	WLAN_CLK_CPU#	>>>	_____
24	WLAN_PCIE_WAKE#	<<<	_____
20,24,62,63	PCIE_WAKE#	<<<	_____
24	WLAN_PWR_EN#	>>>	_____
89	PCIE_WAKE#R	<<<	_____
16,89	WLAN_CLKREQ_CPU#	<<<	_____
89	WLAN_RST#	<<<	_____
89	WIFI_RF_EN_CON	<<<	_____
16	SUS_CLK_CPU	>>>	_____
15,89	BT_USB20_P	>>>	_____
15,89	BT_USB20_N	>>>	_____



NON-IOAC



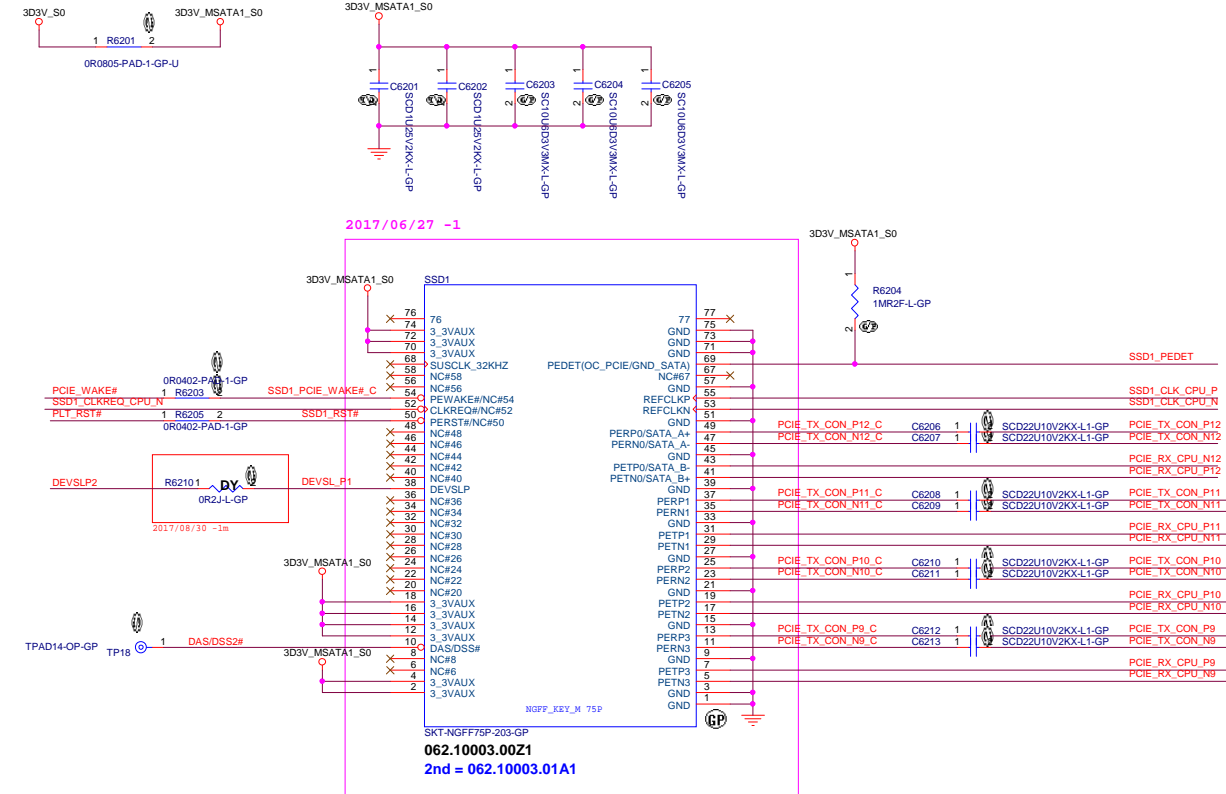
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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

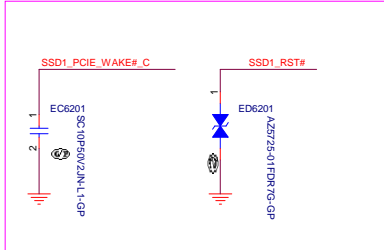
Title			Mini Card-WLAN	
Size	Document Number	Rev		
Custom	Carlsberg_KL	-1M		
Date:	Wednesday, November 01, 2017	Sheet	61	of 106

SSID = mSATA

20,24,61,63 PCIE_WAKE# <<<
16 SSD1_CLKREQ_CPU_N <<<
20,24,61,63,68,89,91 PLT_RST# >>>
15 SSD1_PDET <<<
16 SSD1_CLK_CPU_P >>>
16 SSD1_CLK_CPU_N >>>
15 PCIE_TX_CON_P12 >>>
15 PCIE_TX_CON_N12 >>>
15 PCIE_RX_CPU_N12 >>>
15 PCIE_RX_CPU_P12 >>>
15 PCIE_TX_CON_P11 >>>
15 PCIE_TX_CON_N11 >>>
15 PCIE_RX_CPU_P11 >>>
15 PCIE_RX_CPU_N10 >>>
15 PCIE_RX_CPU_P10 >>>
15 PCIE_TX_CON_N10 >>>
15 PCIE_TX_CON_P10 >>>
15 PCIE_RX_CPU_N9 >>>
15 PCIE_RX_CPU_P9 >>>
15 PCIE_TX_CON_N9 >>>
15 PCIE_TX_CON_P9 >>>
15 DEVSLP2 <<<



2017/06/27 -1



Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

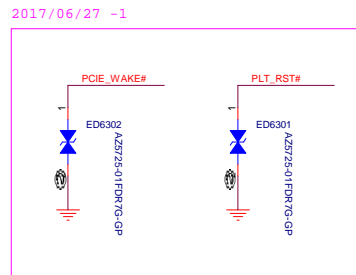
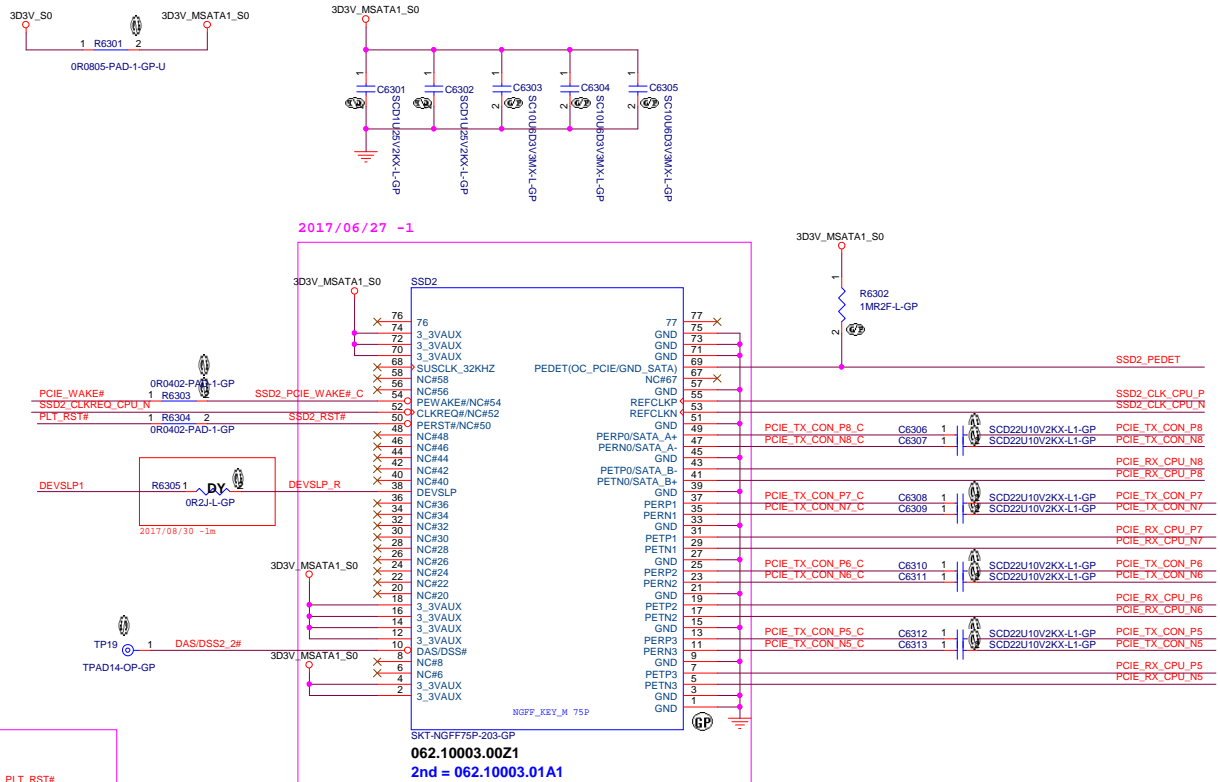
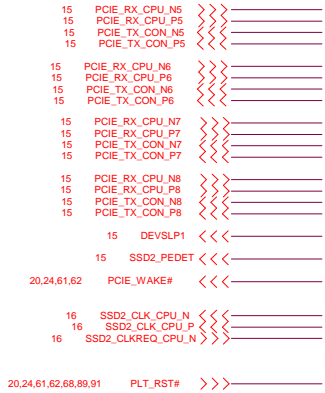
Notes:

- Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraints, Required: Refer Chapter 3, "General Differential Signals Design Guidelines" * along with the additional guidelines in this section for all design optimization guidelines.
- Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices or PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration where the motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichang, Taipei Hsien 221, Taiwan, R.O.C.		
Title SSD1		
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SSID = mSATA



<Core Design>

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Title			
SSD2			
Size	Document Number	Rev	
Custom	Carlsberg_KL	-1M	
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SSID = User.Interface

Blanking

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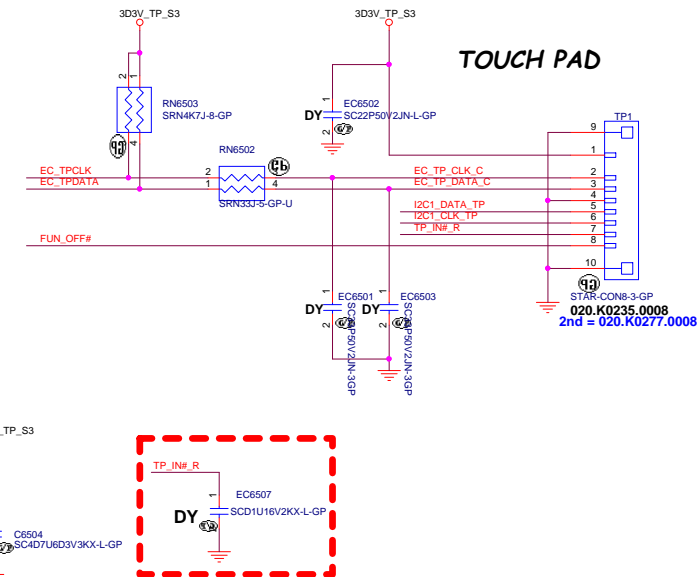
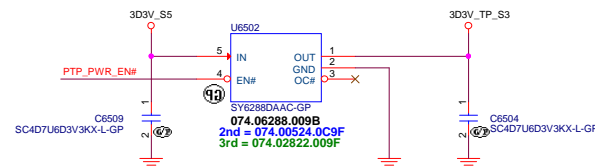
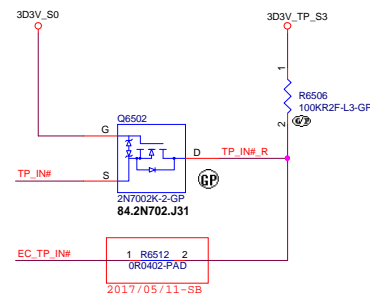
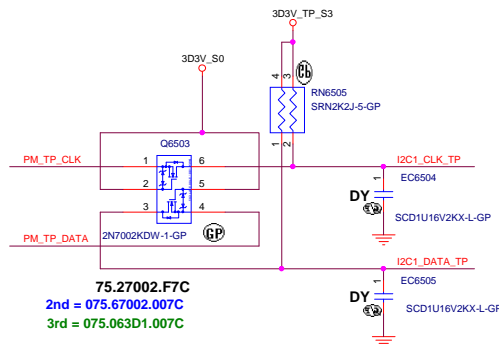
Title **LED Bard/Power Button**

Size Custom	Document Number Carlsberg KL	Rev -1M
Date: Wednesday, November 01, 2017	Sheet 64 of	106

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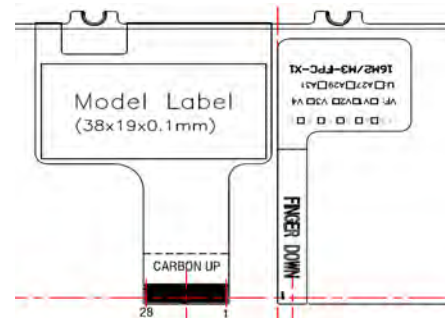
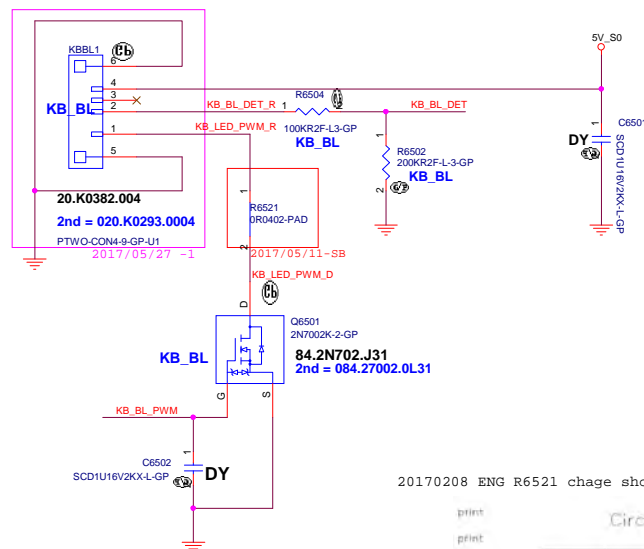
89    EC_TP_CLK_C << >> _____
89    EC_TP_DATA_C << >> _____
89    I2C1_DATA_TP << >> _____
89    I2C1_CLK_TP << >> _____
89    TP_IN#_R << >> _____

```



Internal KeyBoard Connector

24.89	KBC_PWRBTRN#	<<<	<<<
24.89	KS10		
24.89	KS11		
24.89	KS12		
24.89	KS13		
24.89	KS14		
24.89	KS15		
24.89	KS16		
24.89	KS17		
24.89	KS00		
24.89	KS01		
24.89	KS02		
24.89	KS03		
24.89	KS04		
24.89	KS05		
24.89	KS06		
24.89	KS07		
24.89	KS08		
24.89	KS09		
24.89	KS010		
24.89	KS011		
24.89	KS012		
24.89	KS013		
24.89	KS014		
24.89	KS015		
24.89	KS016		
24.89	KS017		



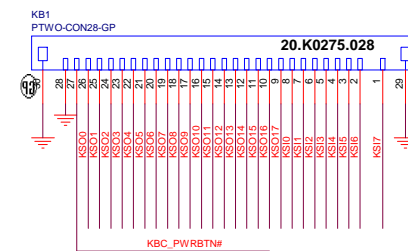
	R01	R02	R03	R04	R05	R06	R07	R08	R09	R10	R11	R12	R13	R14	R15	R16	R17	R18
C06	4	2				4			21	23	21	76	21	22	26	23	23	21
C07	44					62	22	22	23	21	119	21	24	22		76	62	
C06	26					62	119	24	76	73	22	24	22	22	22	21	21	
C05	26	22				22	22	22	22	22	22	22	22	22	22	22	22	
C04	26	26			22	22	22	22	22	22	22	22	22	22	22	22	22	
C03	2				26	2	22	2	2	2	22	22	22	22	22	22	22	
C02	22	44			22	22	2	2	22	22	22	22	22	22	22	22	22	
C01	22	22			22	22	22	22	22	22	22	22	22	22	22	22	22	

PC-402

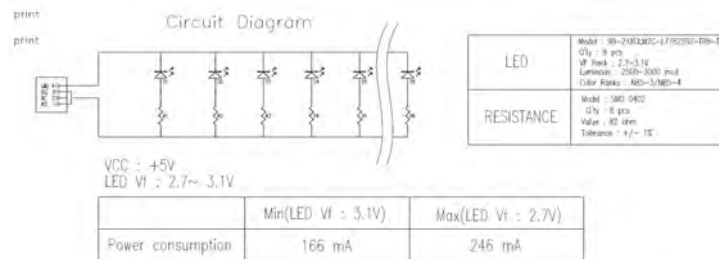
PC-006

VIEW FROM TOP SIDE

PC NUMBER



20170208 ENG R6521 chage short PAD



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	Key Board/Touch Pad
-------	----------------------------

Size	Document Number	Rev
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LED Status

24,89 STDBY_LED >>> _____
 24,89 POWER_LED >>> _____
 24,89 CHARGE_LED >>> _____
 24,89 DC_BATFULL >>> _____

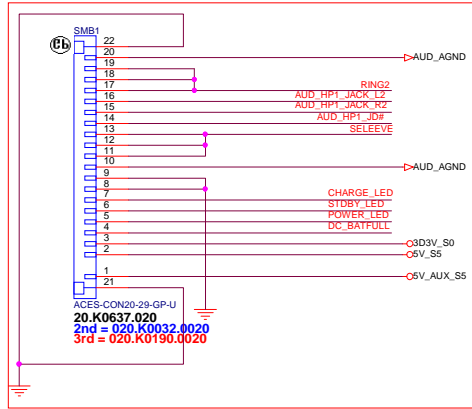
Audio

27,66,89 SELEEVE >>> _____
 27,66,89 AUD_HP1_JACK_L2 <<< _____
 27,66,89 AUD_HP1_JACK_R2 <<< _____
 27,66,89 RING2 >>> _____
 27,66,89 AUD_HP1_JD# >>> _____

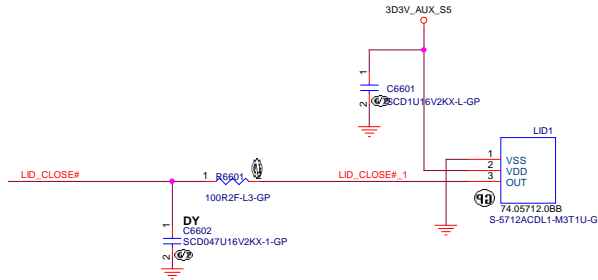
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 27,66,89 AUD_HP1_JACK_R2 <<< _____
 27,66,89 RING2 >>> _____
 27,66,89 AUD_HP1_JD# >>> _____
 89 LID_CLOSE#_1 <<< _____
 24 LID_CLOSE# <<< _____

2017/05/03 -SB
 2017/05/16 - SB change connector pindefine



HALL SENSOR



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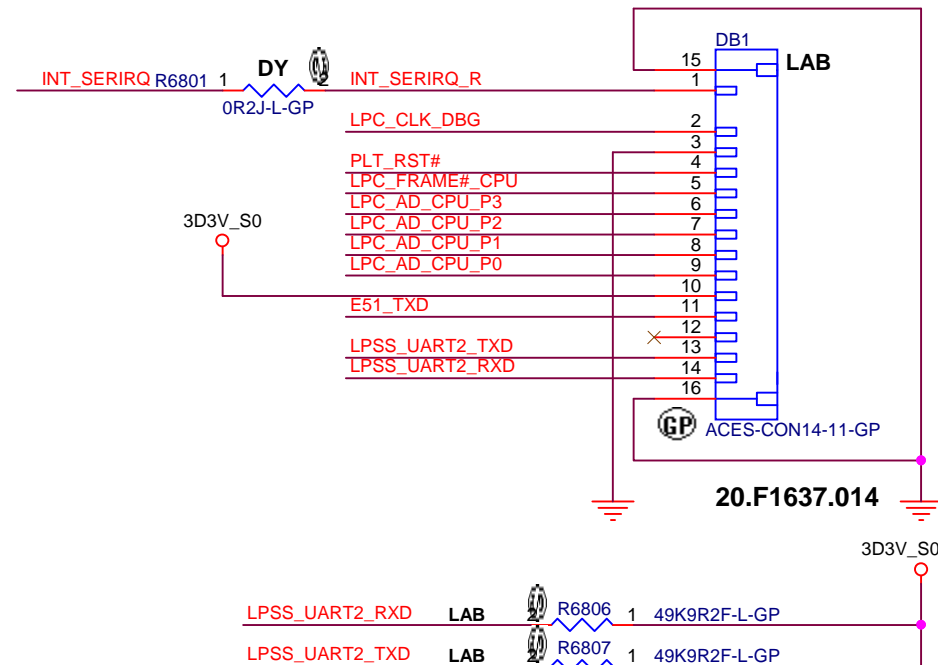
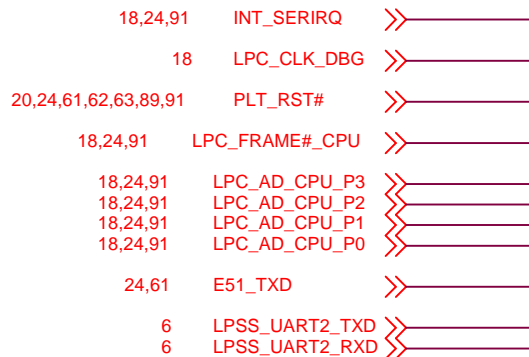
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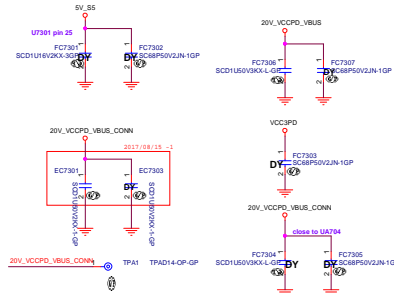
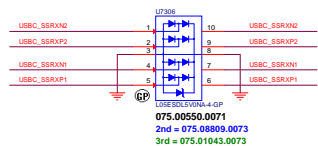
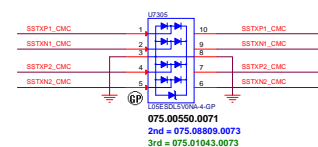
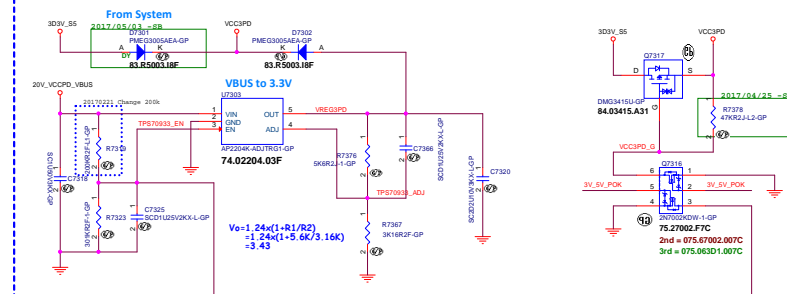
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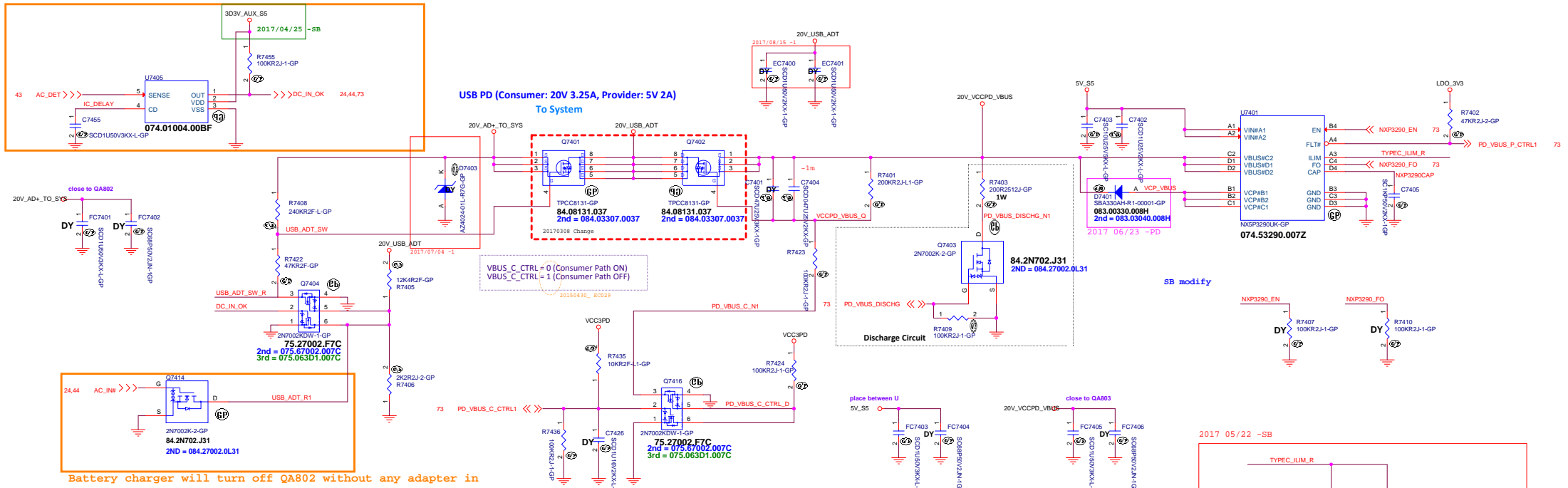
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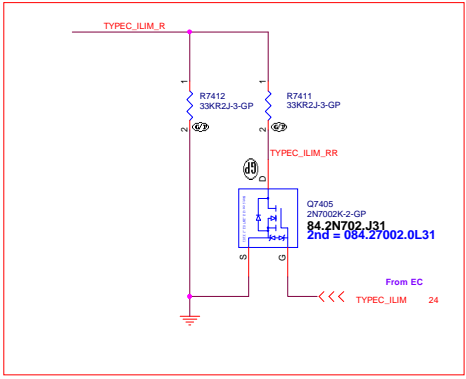
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OTHER





19V Power source type	Control Pin				PMOS Location	Status	Remark
	Net name	Status	Net name	Status			
Normal adapter Only	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	Control by DC_IN_OK
					Q7402	OFF	Control by PD_VBUS_C_CTRL1
					PU4401	ON	
					PU4402	OFF	
Type-C adapter Only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	Low	Q7401	ON	
					Q7402	ON	
					PU4401	OFF	
					PU4402	OFF	
Normal adapter + Type-C	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	
					Q7402	OFF	
					PU4401	ON	
					PU4402	OFF	
Battery only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	High	Q7401	OFF	
					Q7402	OFF	
					PU4401	OFF	
					PU4402	ON	Battery 放電到DCBATOUT



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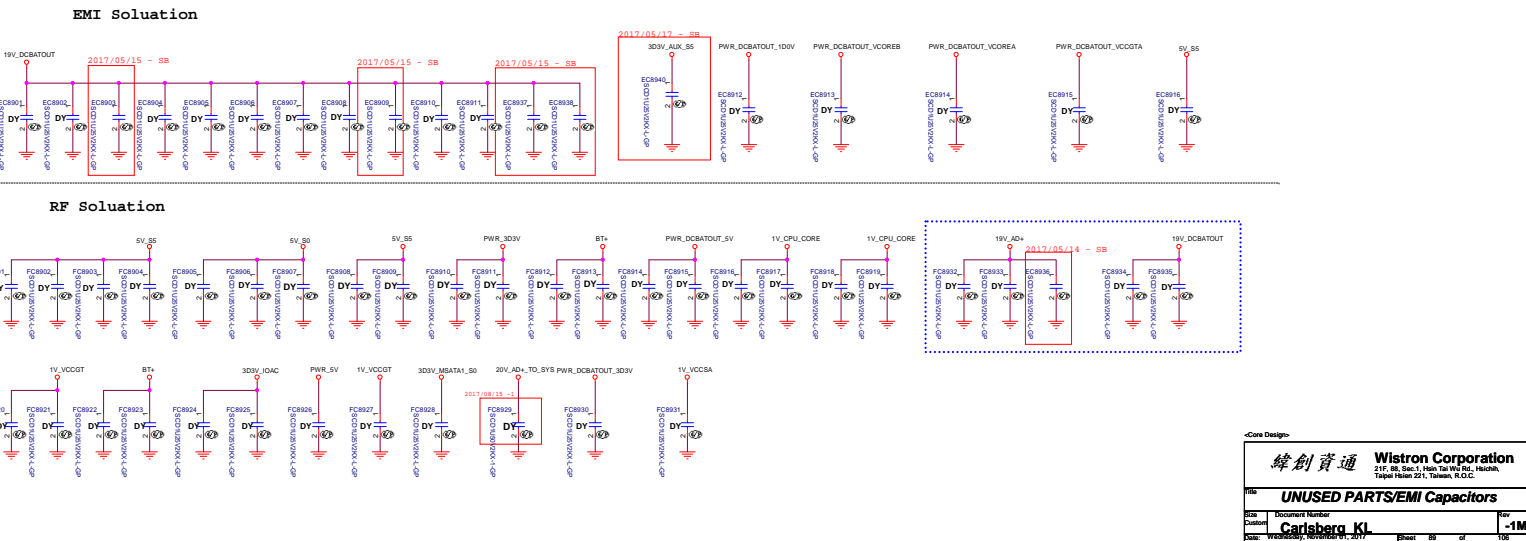
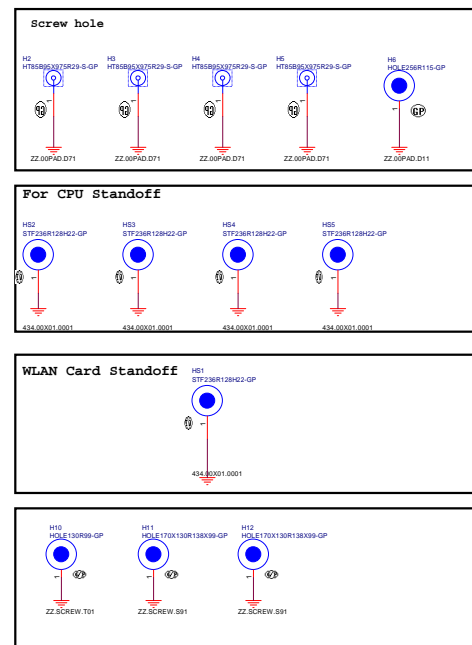
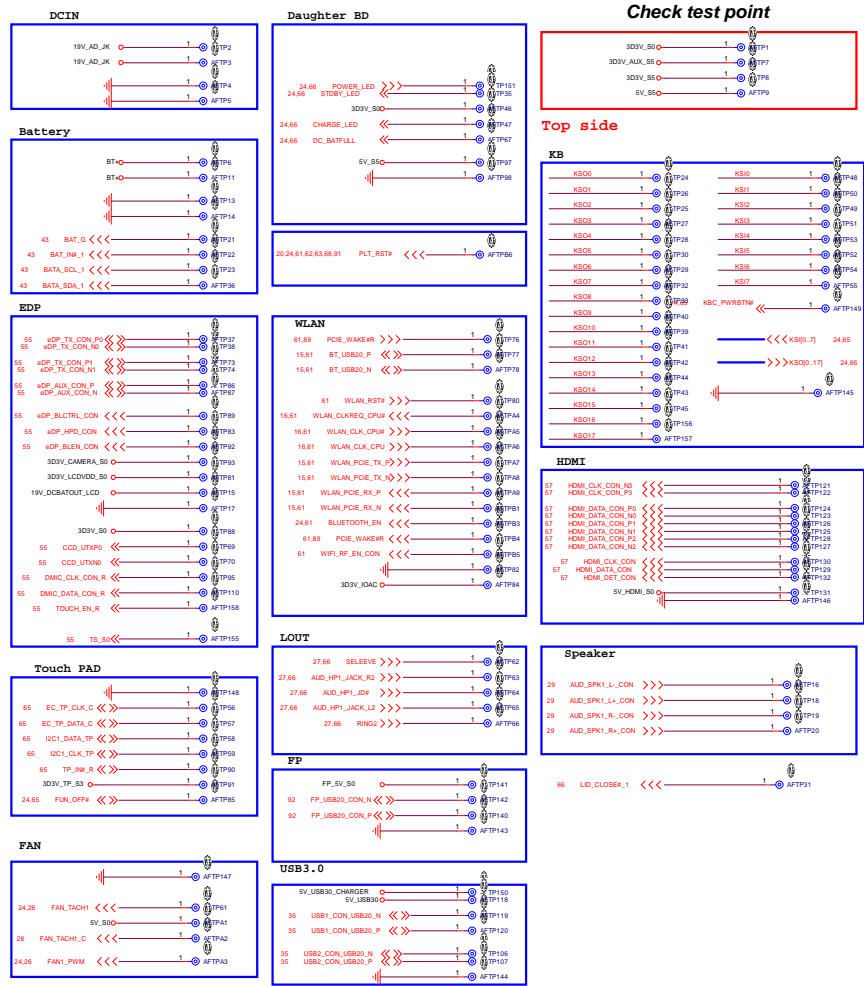
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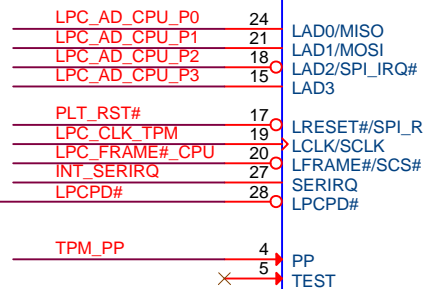
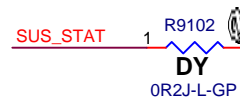
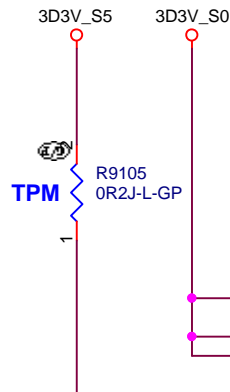
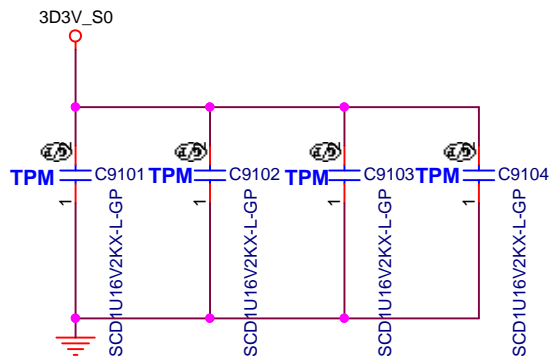
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18,24,68 LPC_AD_CPU_P1 <<<<
18,24,68 LPC_AD_CPU_P2 <<<<
18,24,68 LPC_AD_CPU_P3 <<<<
18 LPC_CLK_TPM <<<
18,24,68 LPC_FRAME#_CPU <<<
20,24,61,62,63,68,89 PLT_RST# <<<<
18,24,68 INT_SERIRQ <<<<
18,24 PM_CLKRUN#_EC <<<<
18 SUS_STAT >>>>

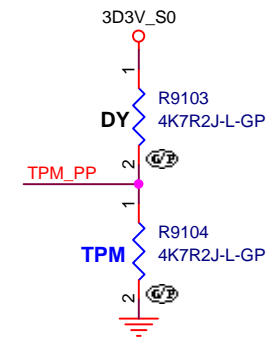


U9101 TPM

NPCT650ABBYX-GP

071.00650.0N03

P/N: 071.00650.0N03



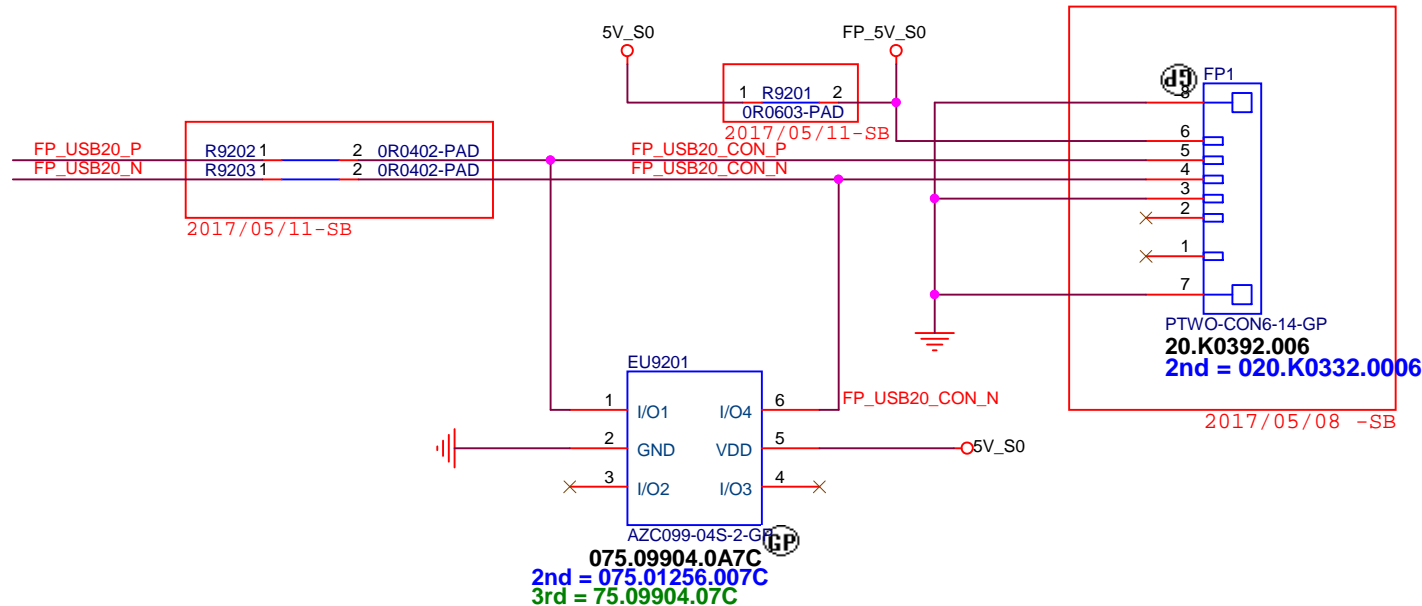
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15 FP_USB20_N << >> _____
15 FP_USB20_P << >> _____

AFTP

89 FP_USB20_CON_N << >> _____
89 FP_USB20_CON_P << >> _____



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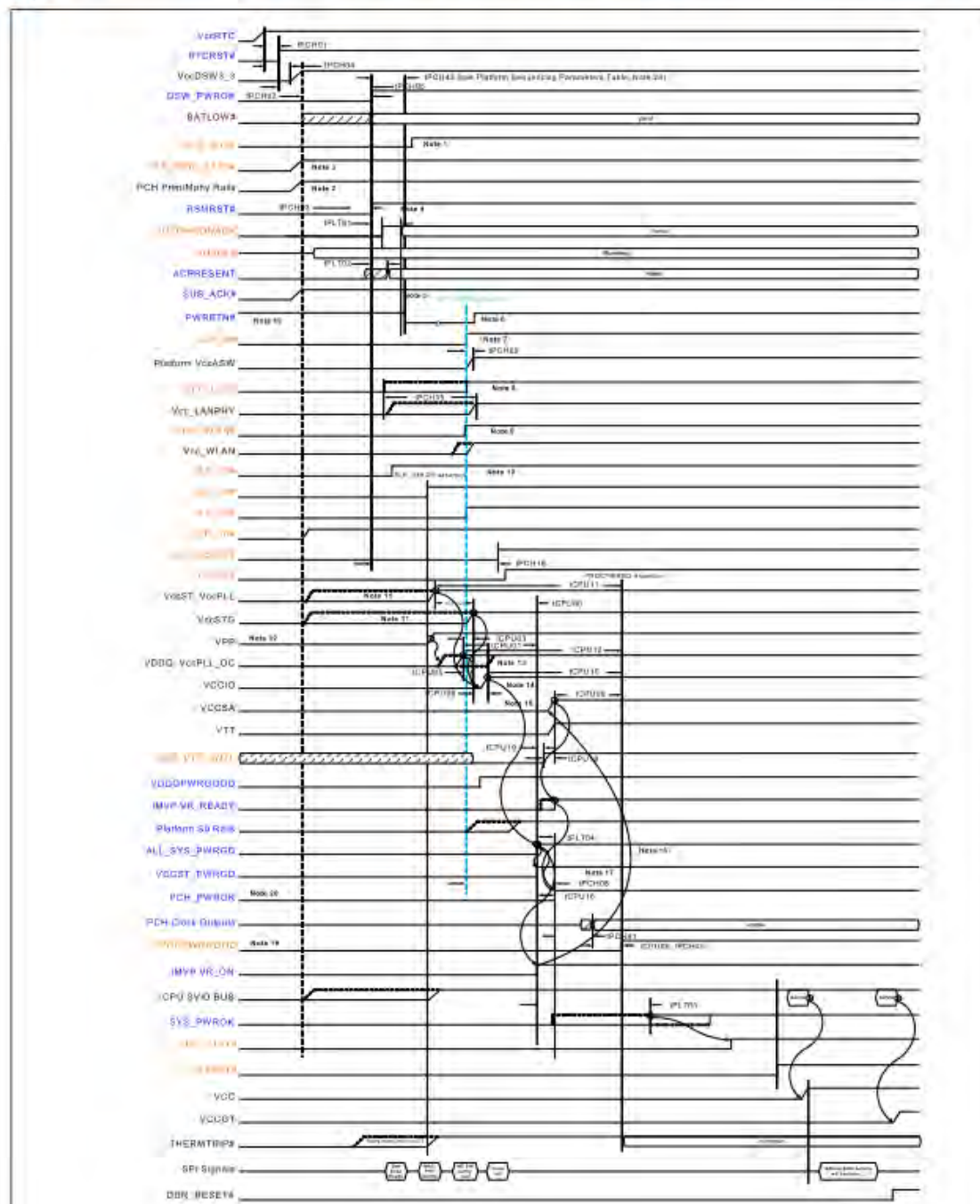
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Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 1 of 2)



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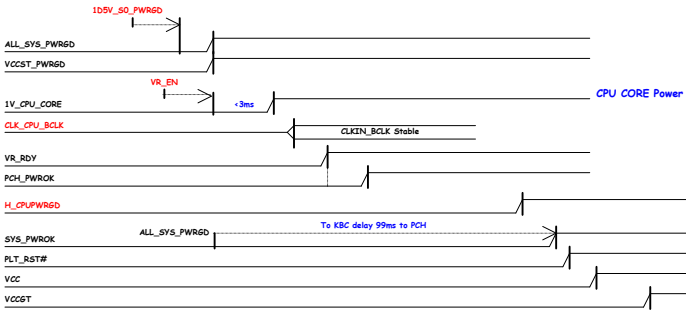
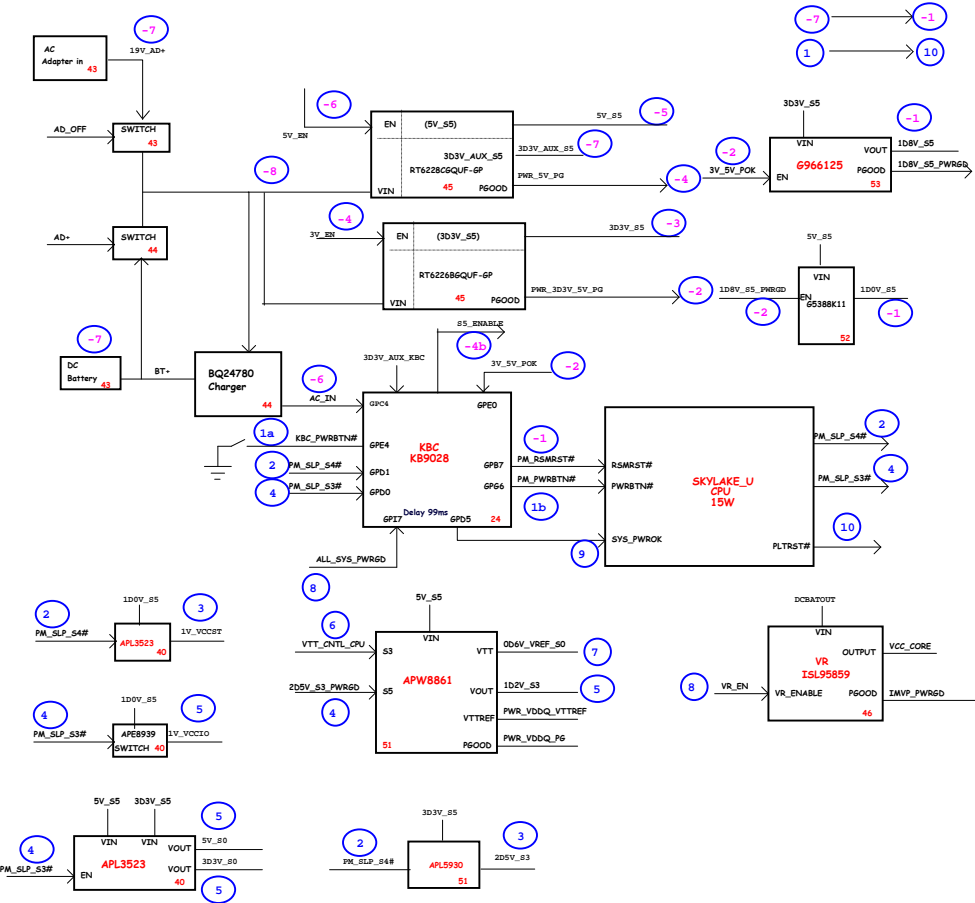
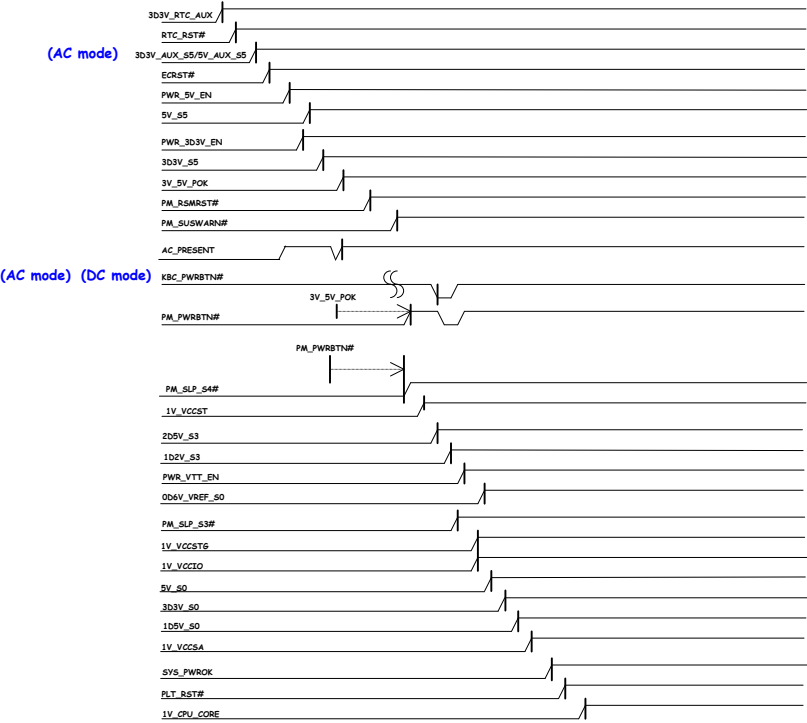
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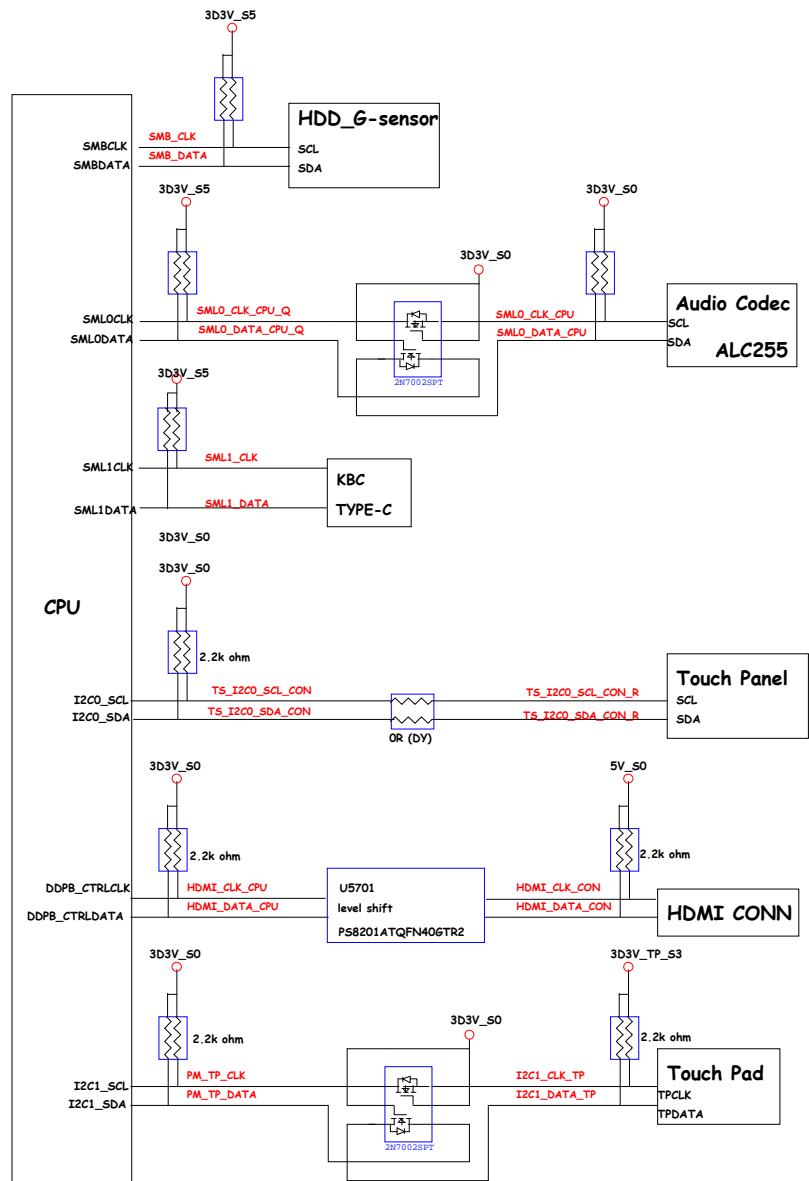
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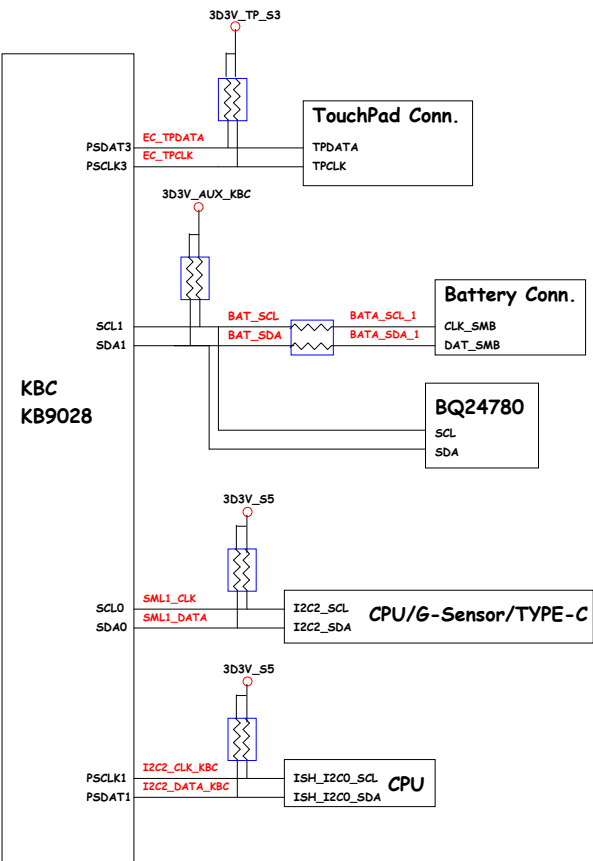
Intel-Power Up Sequence



PCH SMBus/I2C Block Diagram

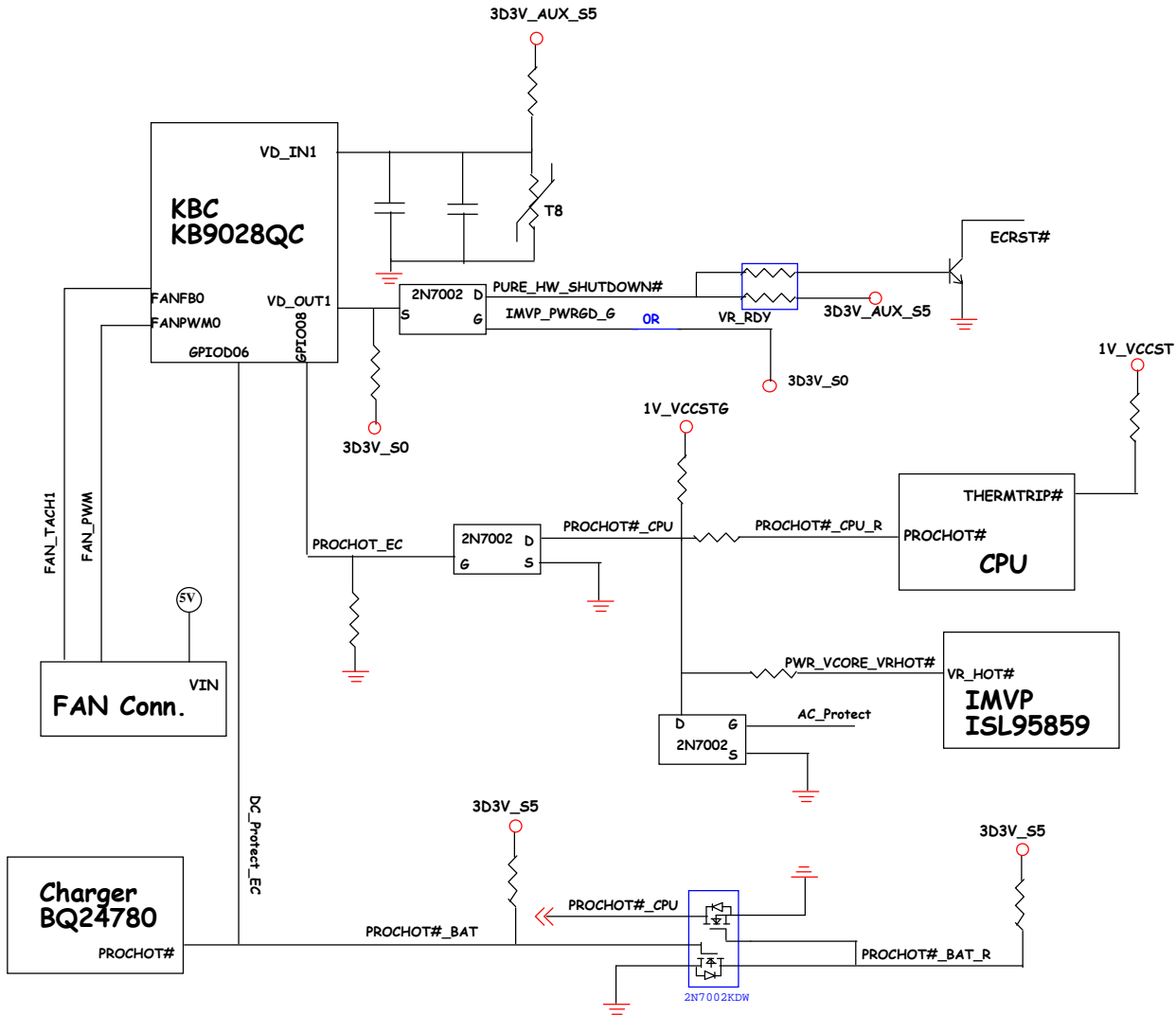


KBC SMBus/I2C Block Diagram

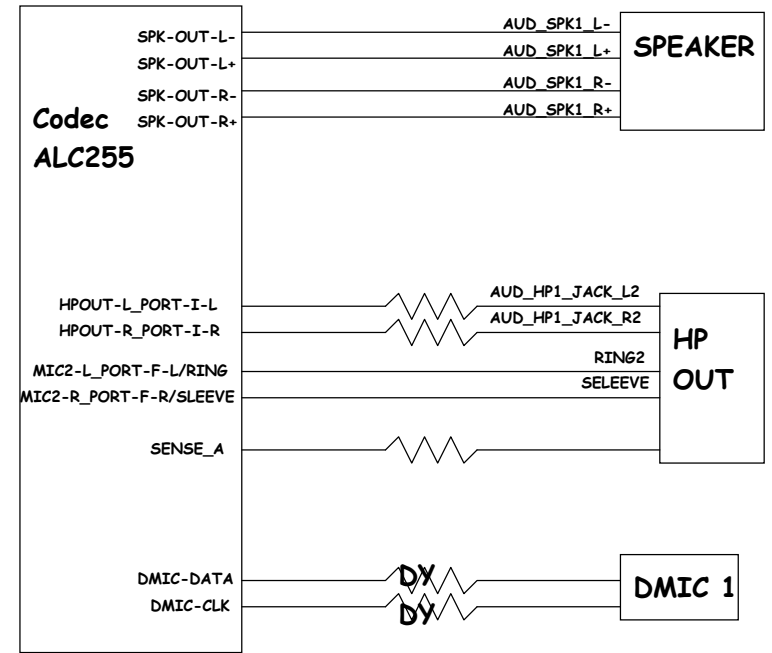


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Thermal Block Diagram



Audio Block Diagram



CLOCK BLOCK DIAGRAM

